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(6) MANUFACTURING METHODS AND TECHNOLOGY ENGINEERING (MMTE) PROGRAM FOR THE ESTABLISHMENT OF PRODUCTION TECHNIQUES FOR HIGH DENSITY THICK FILM CIRCUITS USED IN CRYSTAL OSCILLATORS.

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PREPARED BY

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20. Abstract (cont'd) and flat metal covers, the generation of detailed test flow plans and of preliminary electrical test procedures, the design and fabrication of special tooling and fixturing for hermetic sealing, resistor trimming and electrical testing, the processing of thick film substrates and the start of substrate assembly. Details of this work are reported, and the designs documented herein.

# MANUFACTURING METHODS AND TECHNOLOGY ENGINEERING (MM&TE) PROGRAM FOR THE ESTABLISHMENT OF PRODUCTION TECHNIQUES FOR HIGH DENSITY THICK FILM CIRCUITS USED IN CRYSTAL OSCILLATORS

SECOND QUARTERLY PROGRESS REPORT
22 NOVEMBER 1976 - 27 FEBRUARY 1977
CONTRACT NO. DAAB07-76-C-8119

PREPARED BY
CHARLES T. MARTIN

## OBJECT OF STUDY

The objectives of the program are to establish production techniques for high density thick film hybrid microcircuits used in crystal oscillators and to produce quantities of a 20 MHz temperature-compensated, voltage-controlled crystal oscillator (TCVCXO) using those techniques.

## DISTRIBUTION STATEMENT

## ABSTRACT

Production techniques are being established for a thick film hybrid microelectronic 17-22 MHz, temperature-compensated, voltage-controlled crystal oscillator. In the engineering phase of this program, the following was accomplished during this quarter: the design of a module extraction feature, the detailed design of module potting shells, the generation of master artwork of the thick film circuit patterns, the continued development of a process for hermetically sealing the hybrid microcircuits using ceramic corrals and flat metal covers, the generation of detailed test flow plans and of preliminary electrical test procedures, the design and fabrication of special tooling and fixturing for hermetically sealing, resistor trimming and electrical testing, the processing of thick film substrates and the start of substrate assembly. Details of this work are reported, and the designs documented herein.

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## 1.0 INTRODUCTION

The engineering phase of this manufacturing methods and technology program consists of the following tasks:

1. Electrical breadboard construction
2. Breadboard evaluation
3. Module configuration design
4. Process flow plan generation
5. Hybrid microcircuit parts selection
6. Hybrid microcircuit parts and bonding tools procurement
7. Thick film processing materials
8. Potting shells and encapsulant materials procurement
9. Hybrid microcircuit layout design
10. Layout artwork generation
11. Thick film printing screen procurement
12. Assembly drawing generation
13. Assembly materials procurement
14. Assembly process development
15. Encapsulation process development
16. Hermetic sealing process development
17. Hermetic sealing parts and materials procurement
18. Test flow plan generation
19. Test procedure generation
20. Test fixture design and fabrication
21. Thick film substrate fabrication
22. Substrate assembly (10-lot)
23. Electrical testing of substrate assemblies (pre-seal tests) (10-lot)
24. Hermetic sealing of substrate assemblies (10-lot)
25. Leak testing of hermetically sealed substrate assemblies (10-lot)
26. Module assembly (10-lot)
27. Electrical testing of assembled modules (pre-aging) (10-lot)
28. Module aging (10-lot)
29. Electrical testing of modules (final tests) (10-lot)
30. Substrate assembly (15-lot)
31. Electrical testing of substrate assemblies (pre-seal tests) (15-lot)

32. Hermetic sealing of substrate assemblies (15-lot)
33. Leak testing of sealed substrate assemblies (15-lot)
34. Module assembly (15-lot)
35. Electrical testing of assembled modules (pre-pot tests) (15-lot)
36. Module encapsulation (15-lot, as required)
37. Electrical testing of encapsulated modules (post-pot tests) (15-lot, as required)
38. Module aging (15-lot)
39. Electrical testing of modules (final tests ) (15-lot)

The 10-lot and 15-lot refers to the two lots of deliverable engineering samples.

During the first quarter of this program, work was performed on tasks 1 - 9, 12, 13 and 17, with tasks 1, 4, 5, 7, 12, and 13 having been completed during that quarter. During the current quarter, work was performed on tasks 3, 8 - 11 and 16 - 22. Details of this work are covered in this report. For discussion purposes in this report, the work is grouped into four categories: design, process development, fixturing/tooling and manufacturing.

## 2.0 MICROCIRCUIT AND MODULE DESIGN

This section covers the work performed on the following tasks:

Task no. 3 - Module configuration design

Task no. 9 - Hybrid microcircuit layout design

Task no. 10 - Layout artwork generation

### 2.1 Module Configuration Design

Subsequent to the completion of the module configuration design [Ref. 1], a requirement arose for the incorporation into the design of two new features: (1) a provision for extracting the module from its socket where essentially only the end of the module opposite to the socket is accessible and (2) protection of the frequency-adjust potentiometer adjustment screw from moisture.

The requirements for an extraction means stems from the fact that the cylindrically shaped module, in its system application, seats snugly in a hole, at the bottom of which is located the socket. The sides of the module are not accessible for grasping with the fingers to extract the module from its socket. Consequently, a provision for module extraction was developed involving the combined use of T-shaped slots in the potting shell exterior surface (fig. 2-1) and a special extraction tool (fig. 2-2). One of the slots has been designed so that, in an emergency, the module will be extractable with the aid of a simple bent wire hook.

The moisture protection feature for the potentiometer screw has not yet been worked out in detail, but it is envisioned that a nylon screw will be used to plug the access hole in the potting shell when potentiometer adjustments are not being made.

### 2.2 Hybrid Microcircuit Layout Designs

During the first quarter, the layout designs were completed for the two TCVGXO hybrid types: the temperature-compensation function generator (TCFG) and the voltage-controlled crystal oscillator (VCXO). The assembly drawing for each was presented in the first quarterly report [ref. 2]. During the second quarter, these designs were reviewed by ECOM, and drawings generated of the thick film screen-printed substrate patterns. These are shown in figures 2-3 and 2-4.

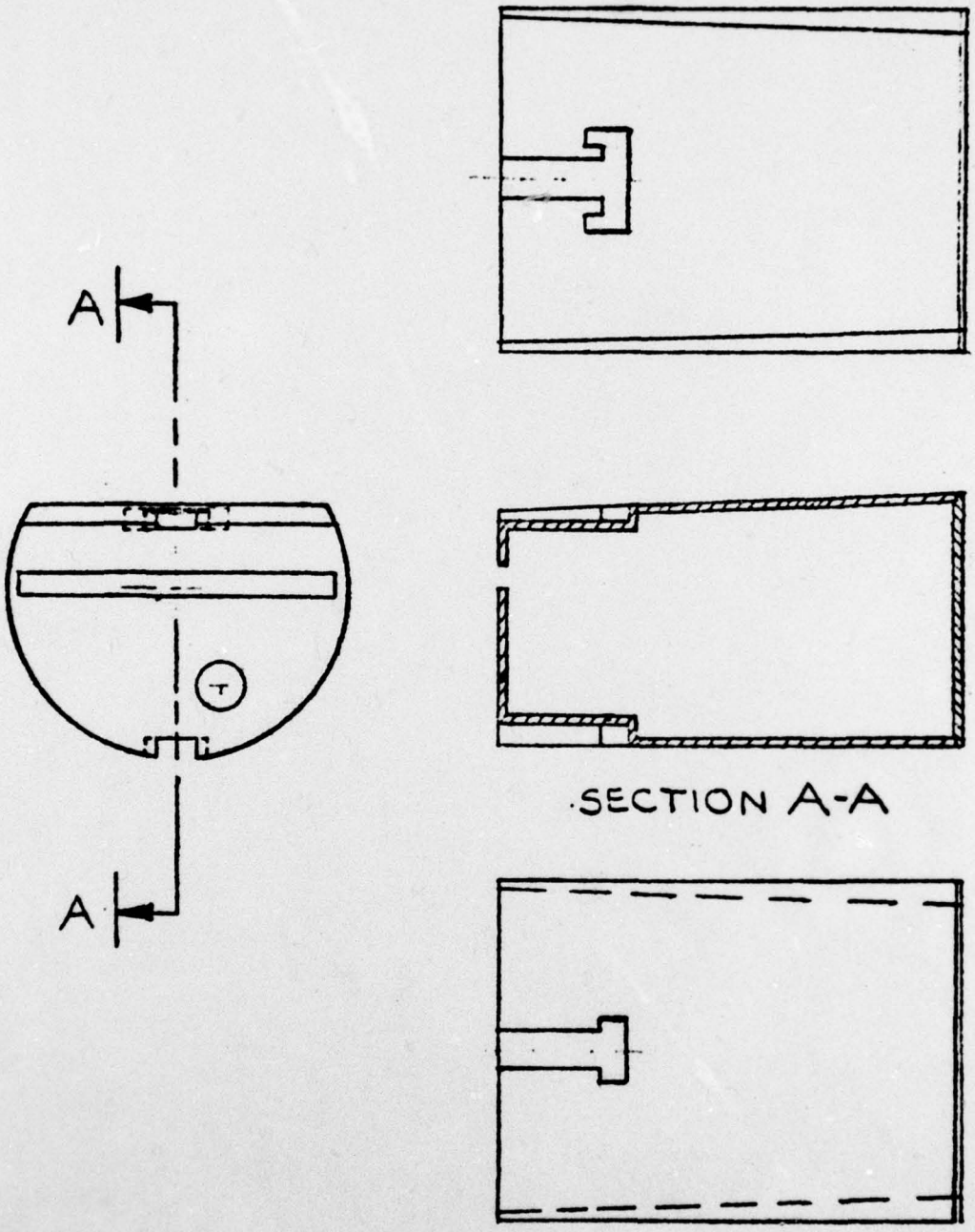



Figure 2-1. Extraction Feature in Potting Shell

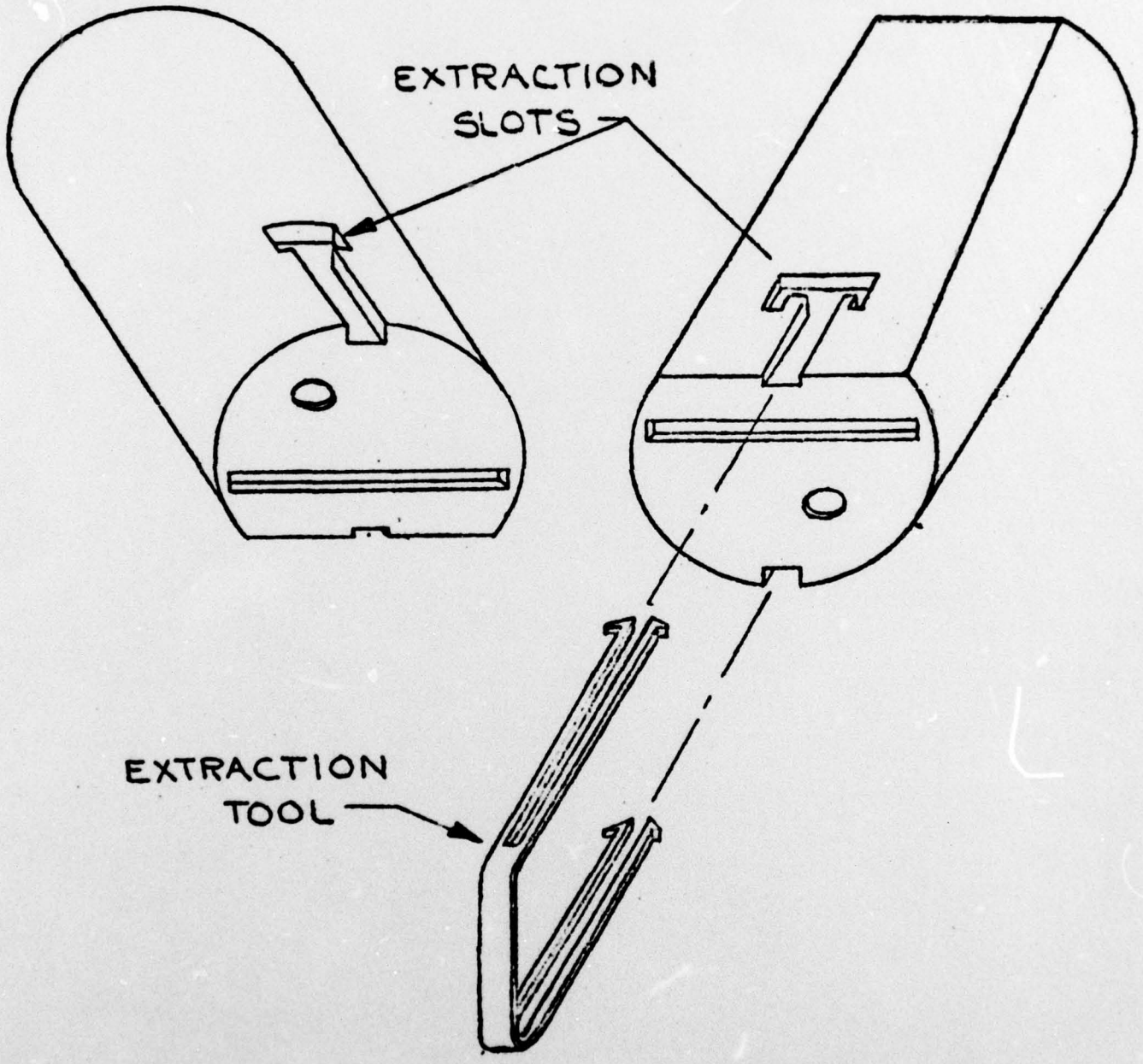



Figure 2-2. Extraction Tool

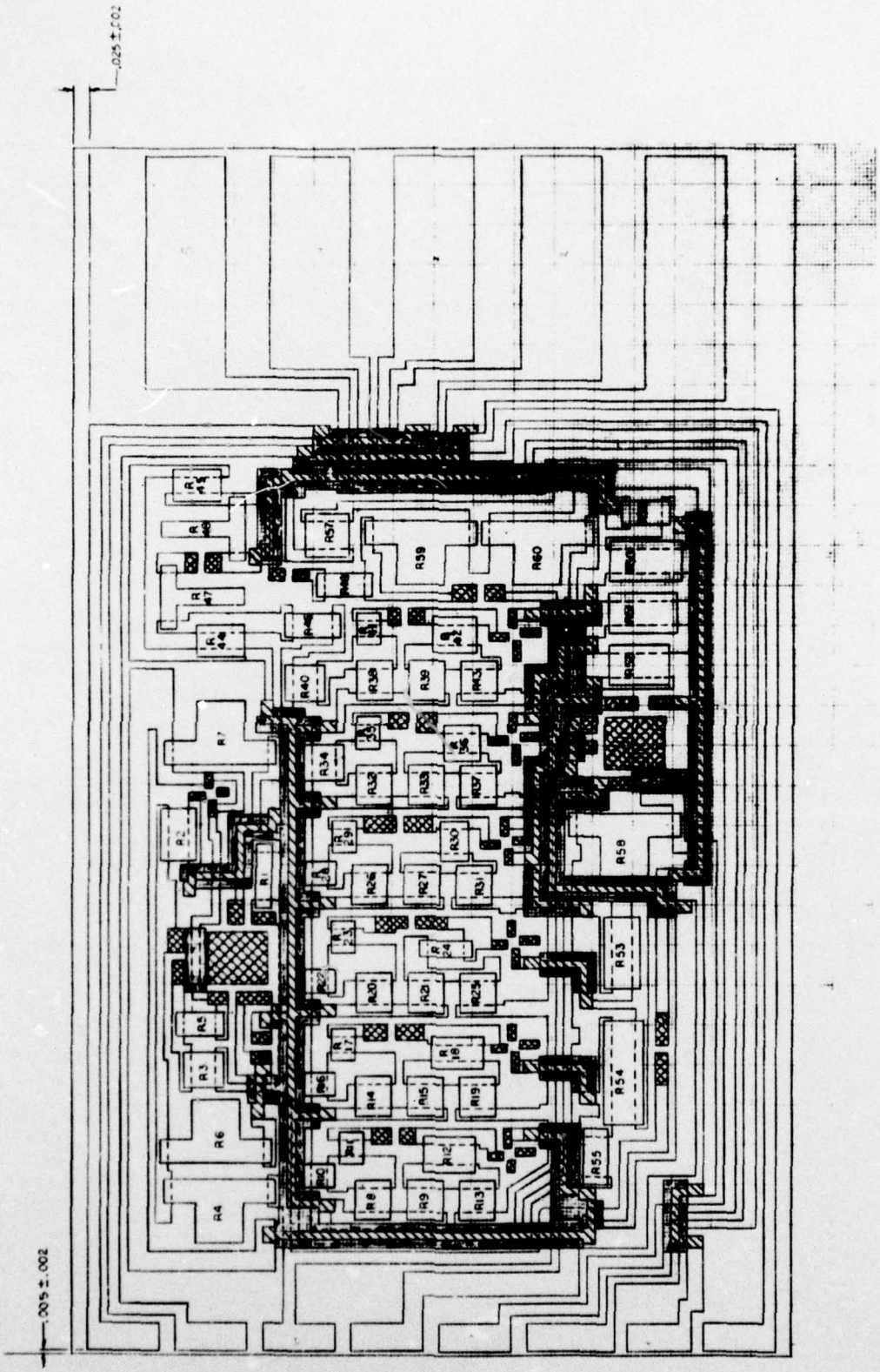



Figure 2-3. TCFG Screened Substrate Drawing

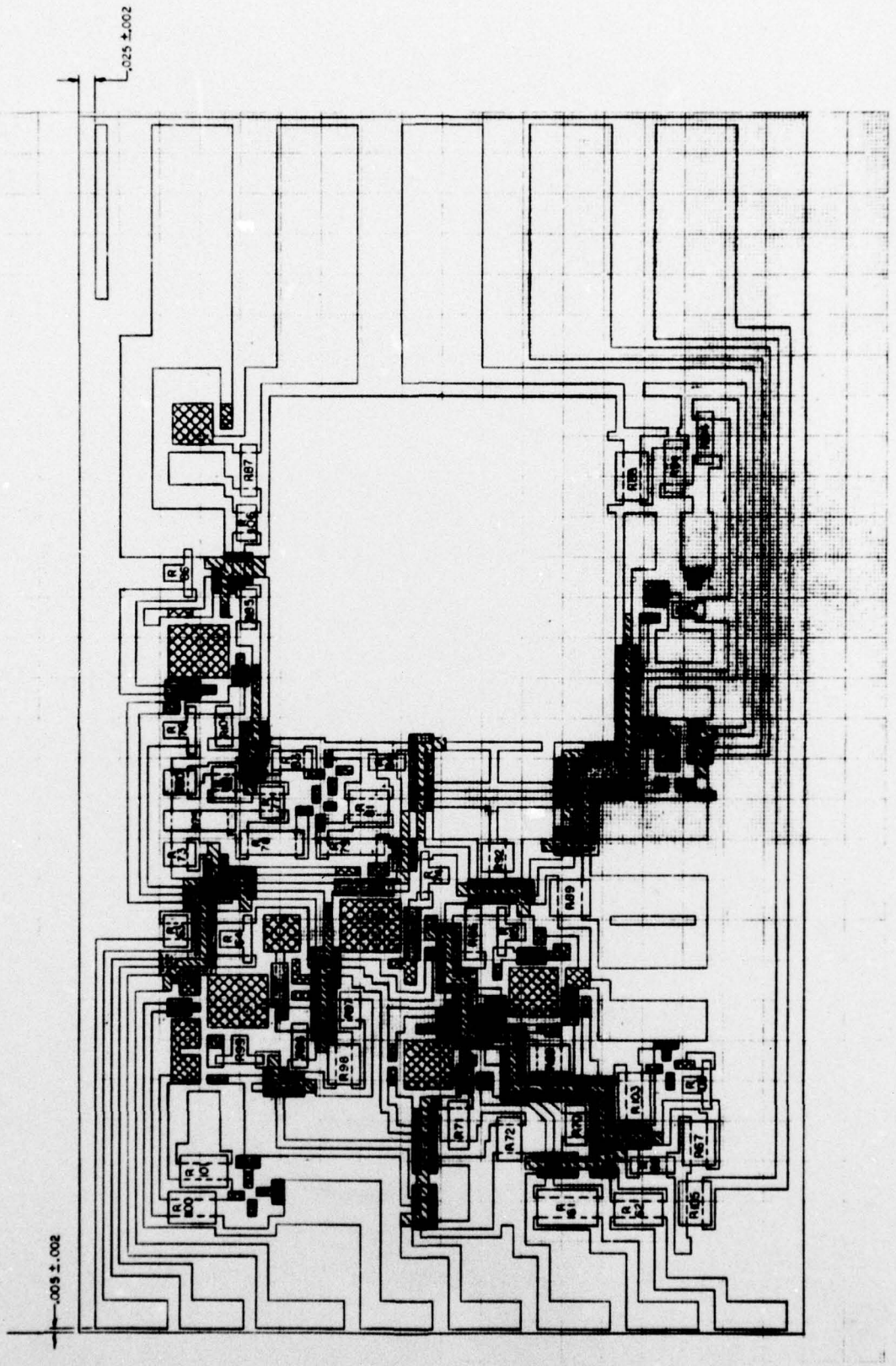



Figure 2-4. VCXO Screened Substrate Drawing

## 2.3 Artwork Generation

The master artwork for the thick film patterns to be printed on the ceramic substrates were machine-generated in Raytheon's Automated Drafting Center. The procedure was to first prepare a so-called "digitizable" layout drawings, showing line widths and routings symbolically. The design information on the color-coded digitizable drawings was then transferred through man-machine interface onto a magnetic tape, and the tape used to drive a photo-plotter. A piece of artwork was photo-plotted on film at 5X scale for each of the thick film conductor and resistor patterns comprising the designs. For each hybrid type, seven sheets of artwork were generated as follows:

Sheet no. 1 - first conductor
Sheet no. 2 - dielectric insulator
Sheet no. 3 - first conductor overlay
Sheet no. 4 - second (crossover) conductor
Sheet no. 5 - resistor, 3KΩ/□
Sheet no. 6 - resistor, 30KΩ/□
Sheet no. 7 - resistor, 300KΩ/□

Figures 2-5 through 2-11 depicts the seven artwork patterns for the TCFG hybrid, and figures 2-12 through 2-18 for the VCXO hybrid. The concept of a digitizable layout drawing is illustrated in figure 2-19 for the VCXO hybrid.

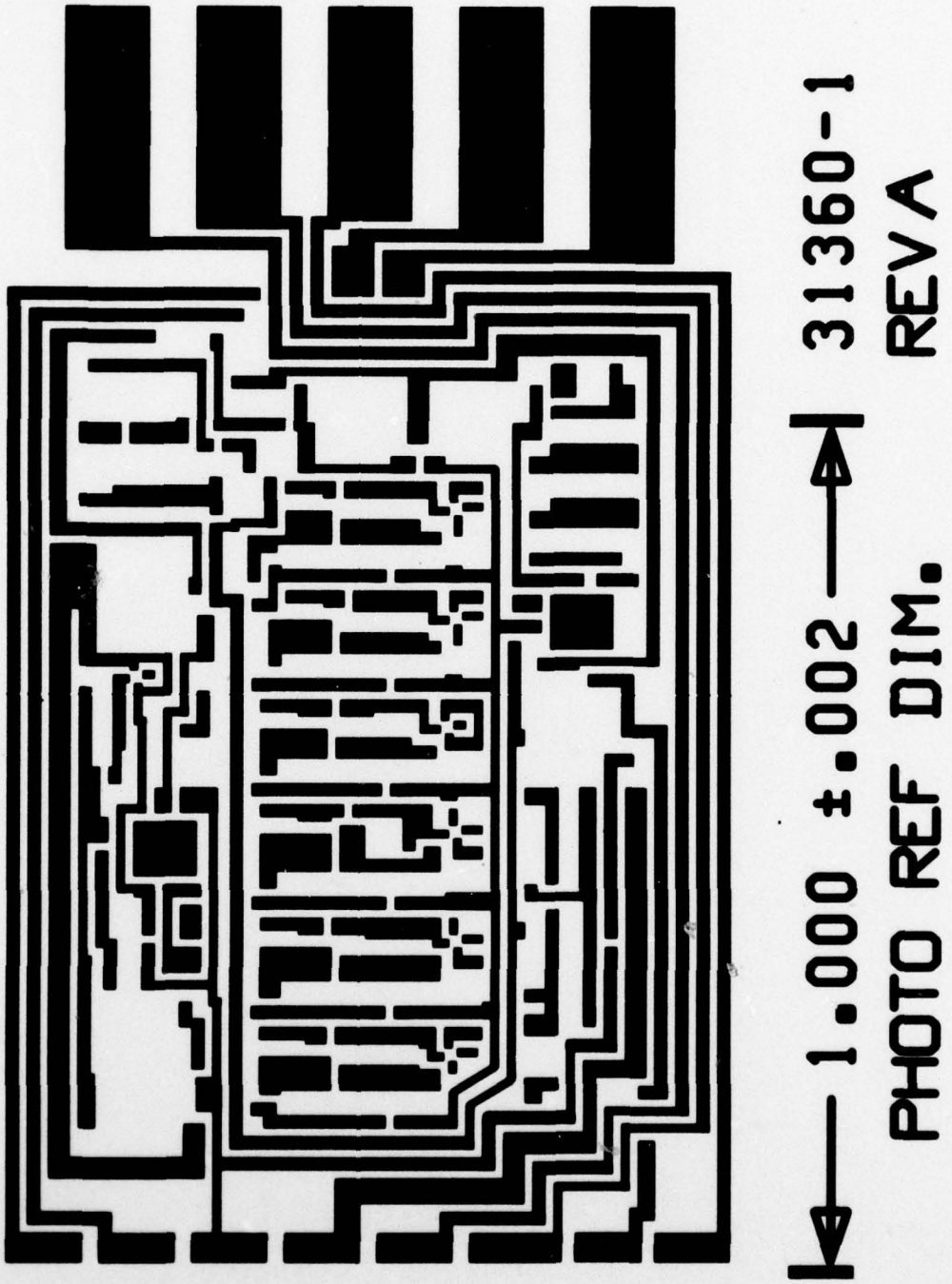



Figure 2-5. TCFG Artwork - First Conductor Pattern

Figure 2-6. TCFG Artwork - Dielectric Insulator Pattern

Figure 2-7. TCFG Artwork - First Conductor Overlay Pattern

Figure 2-8. TCFG Artwork - Second Conductor (Crossover) Pattern

Figure 2-9. TCFG Artwork - Resistor Pattern, 3K ohms per Square

Figure 2-10. TCFG Artwork - Resistor Pattern, 30K ohms per Square

Figure 2-11. TCFG Artwork - Resistor Pattern, 300K Ohms per Square

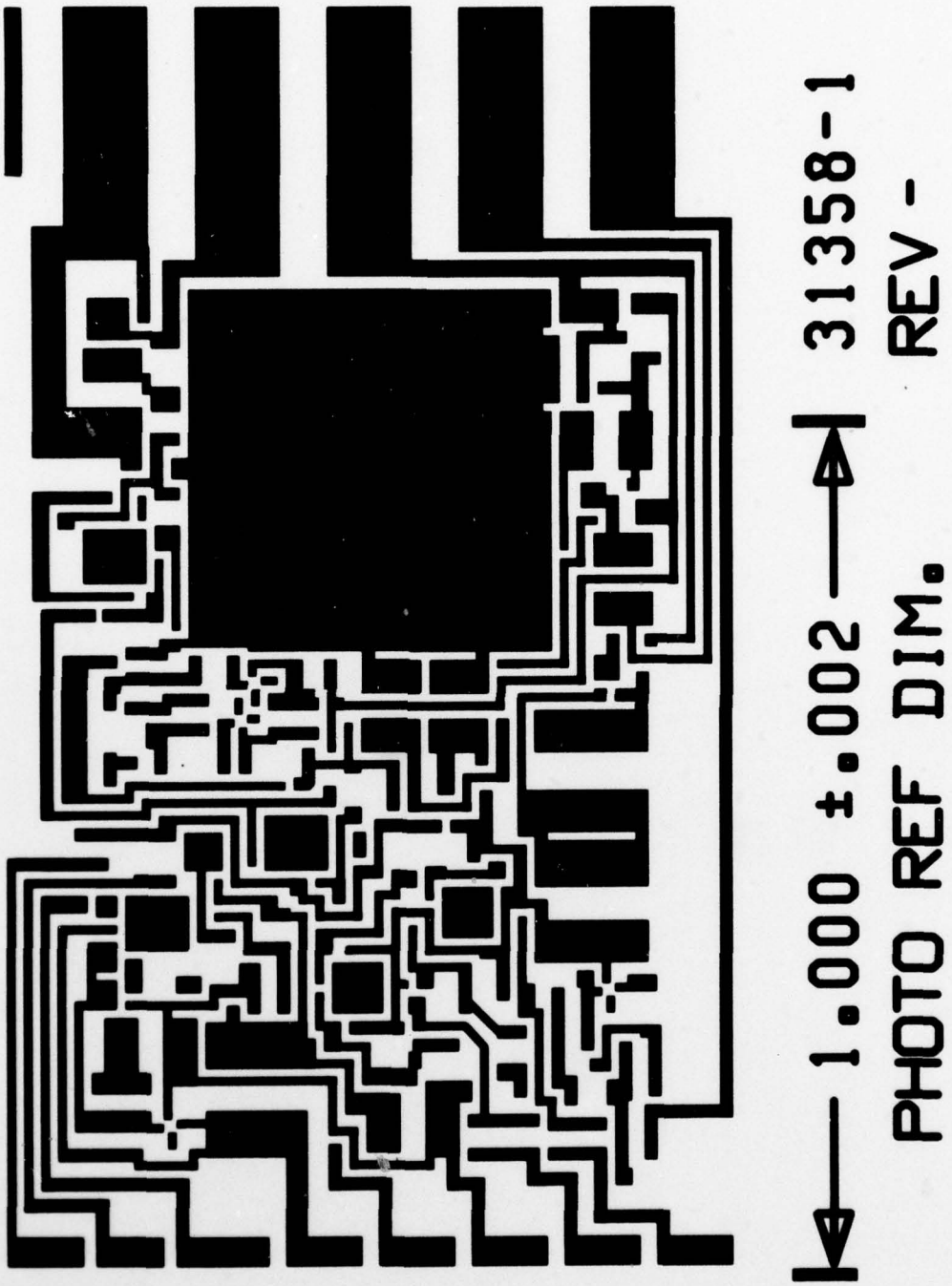



Figure 2-12. VCXO Artwork - First Conductor Pattern

Figure 2-13. VCXO Artwork - Dielectric Insulator Pattern

Figure 2-14. VCXO Artwork - First Conductor Overlay Pattern.

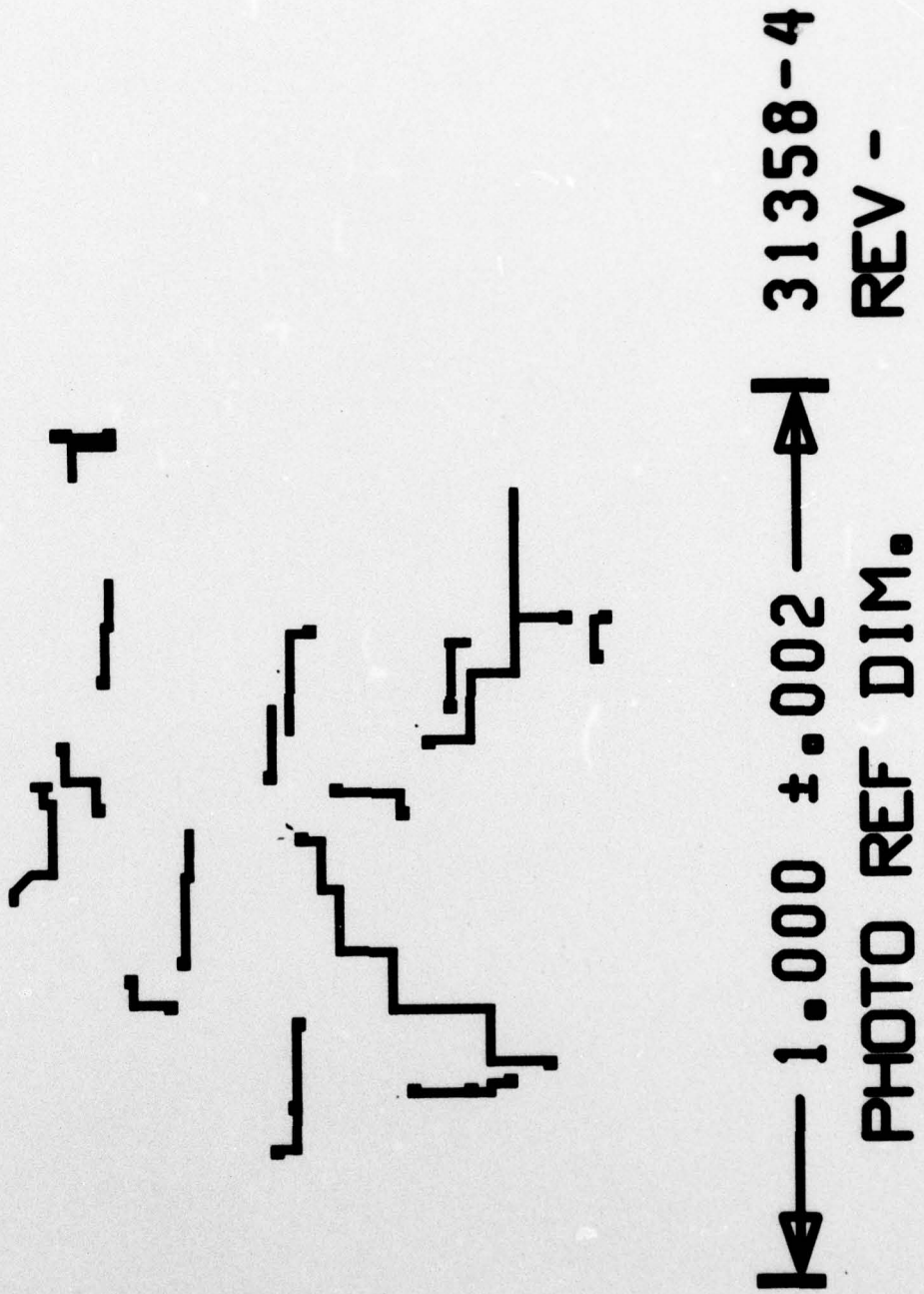



Figure 2-15. VCXO Artwork - Second Conductor (Crossover) Pattern

Figure 2-16. VCXO Artwork - Resistor Pattern, 3K Ohms per Square

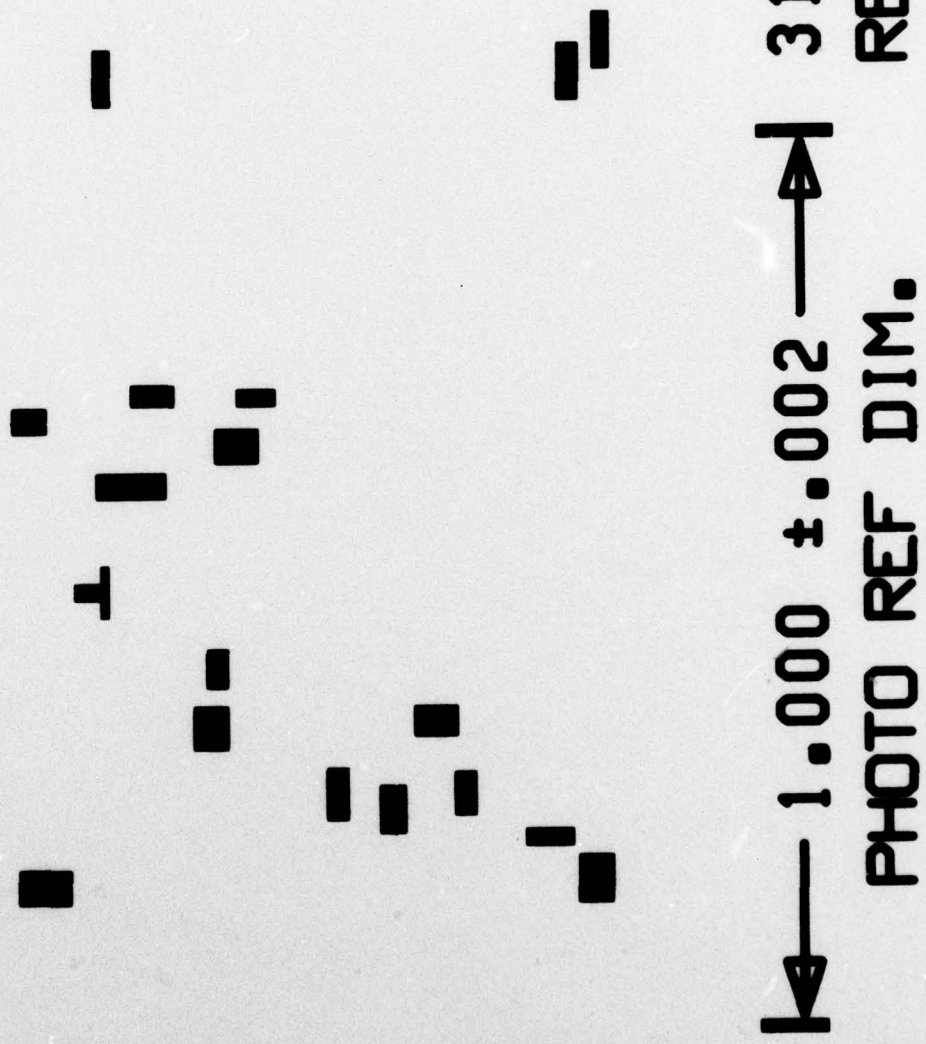
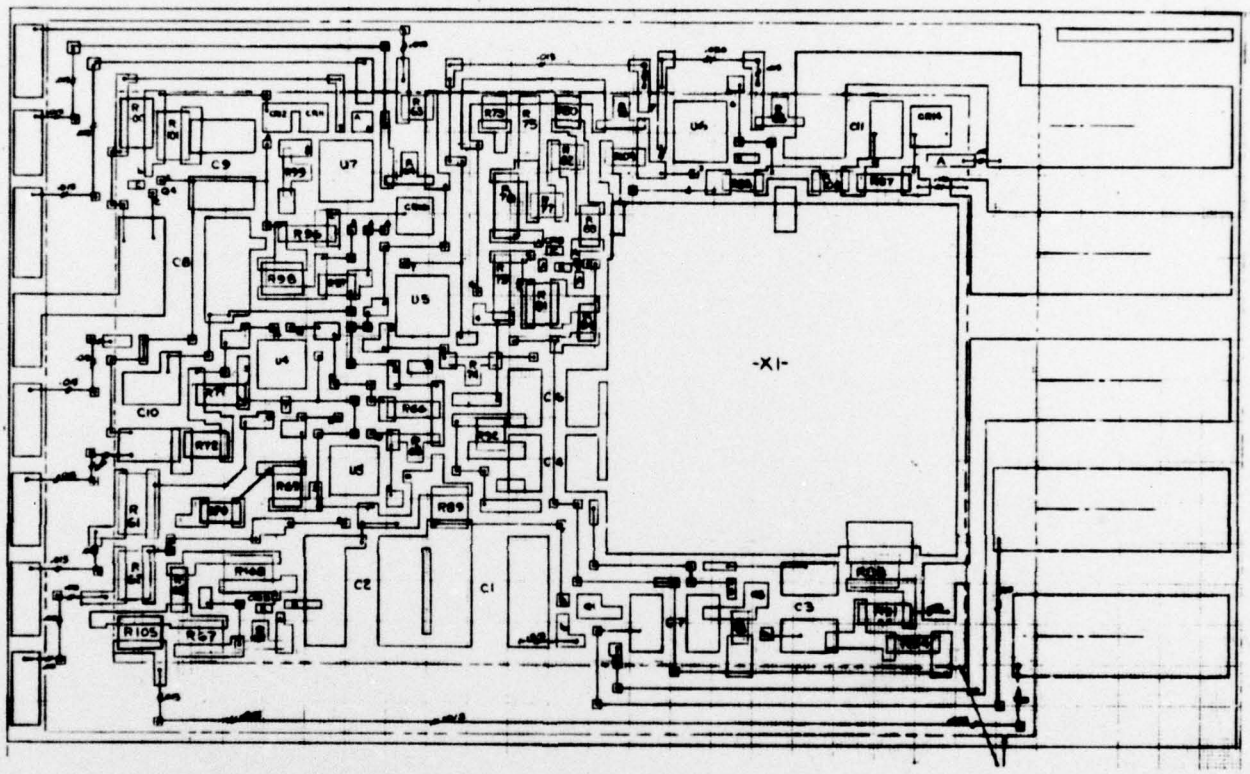



Figure 2-17. VCXO Artwork - Resistor Pattern, 30K Ohms per Square

Figure 2-18. VCXO Artwork- Resistor Pattern 300K Ohms per Square




SHEET 1 OF LAYOUT SHOWING FIRST CONDUCTOR AND 3 RESISTOR PATTERNS ONLY.

**Figure 2-19. Digitizable Layout - VCXO Hybrid**

## 3.0 PROCESS DEVELOPMENT

This section covers the work performed on the following tasks:

Task no. 8 - Potting shell and encapsulation material procurement

Task no. 16- Hermetic sealing process development

Task no. 17- Hermetic sealing parts and materials procurement

Task no. 18- Test flow plan generation

Task no. 19 -Test procedure generation

### 3.1 Potting Shell and Encapsulation Material

The detailed design of the potting shell, to be used in encapsulating the TCVCXO modules, was completed and is shown in figures 3-1 and 3-2. The shell will be transfer molded from short-glass-fiber-filled, black diallyl phthalate, per MIL-M-14F. The particular material to be used is U.S. Polymeric, USP612F. The basic external features and dimensions of the potting shell conform to requirements of ECOM Technical Requirements SCS-483 [ref. 3], as modified [ref. 4]. The potting shell approach was chosen for two reasons over the alternatives of transfer molding or casting to shape the entire module assembly. First, the complex external shape of the module will cause a yield loss in fabrication, and consequently, it is more cost effective to incur this loss in an empty potting shell than in a complete, functioning electronic assembly. Secondly, the module weight specification precludes the use of dense casting or molding resins. A potting shell provides a hard, dense skin for the module that, in turn, provides chemical and handling protection to the assembly and, at the same time, permits the bulk of the encapsulation materfial to be a low-density foam, thus minimizing weight.

### 3.2 Hermetic Sealing Process Development, Parts and Materials

The hermetic sealing process consists first of fabricating a corral assembly, then glass sealing that corral assembly to the thick film substrate and finally, parallel-seam welding a flat metal cover to the top of the corral assembly. Fabricating the corral assembly involves brazing (at about 800°C) a metal (Kovar) frame to a metallized ceramic (alumina) corral so as to render the corral weldable. After brazing, the exposed metal surfaces of the assembly are gold-plated

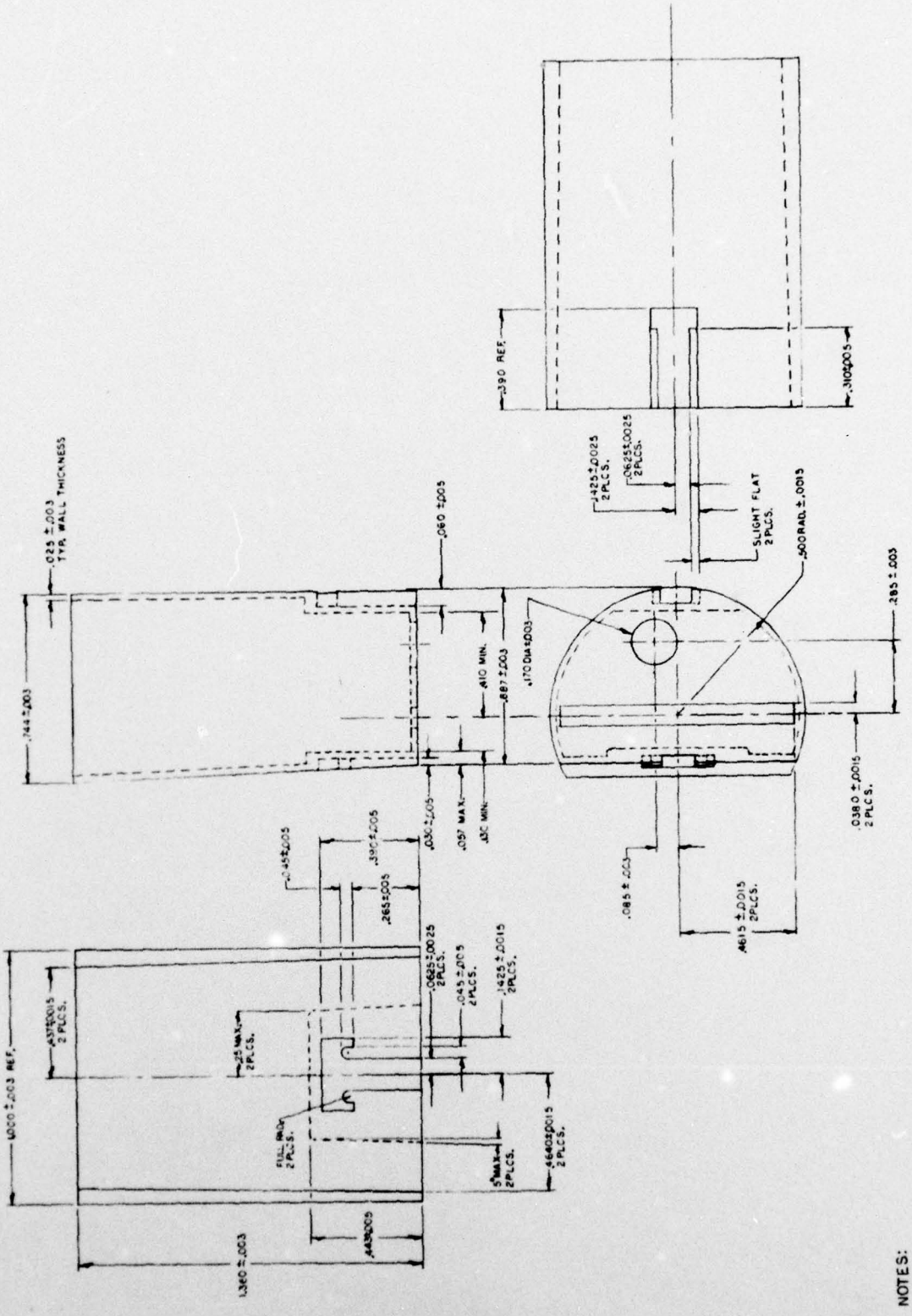



**Figure 3-1. Potting Shell**

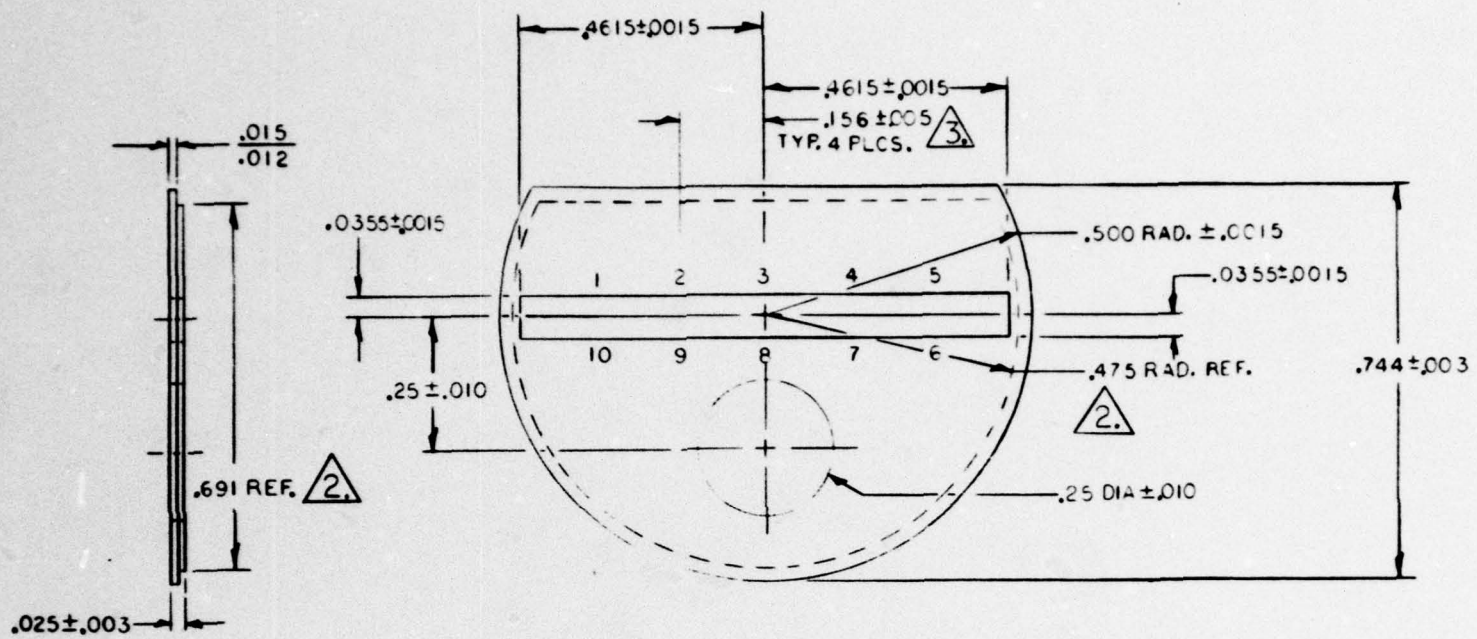



Figure 3-2. Potting Shell Cover

NOTES:

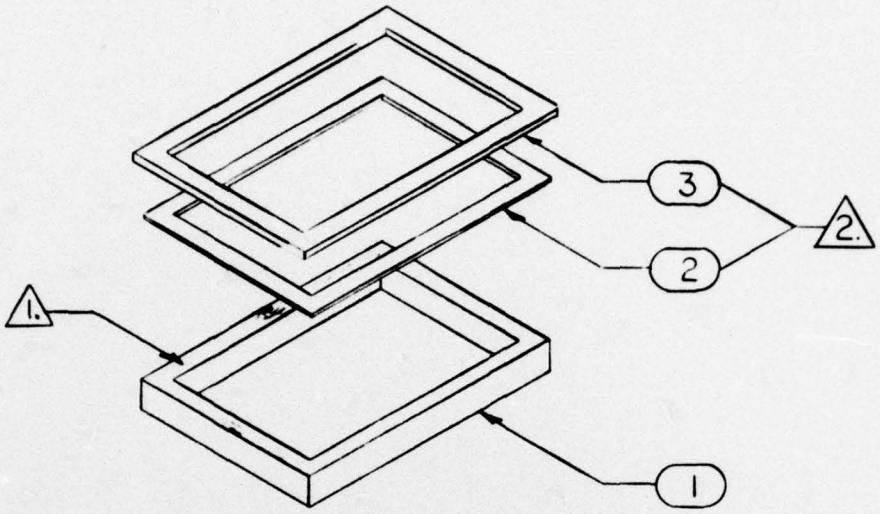
1. MATERIAL: DIALLYL PHTHALATE
2. LIGHT PRESS FIT INTO MATING POTTING SHELL, DWG. NO. 31378
3. TOTAL TOLERANCE NON-ACCUMULATIVE, .156 DIMENSION TO LOCATE RAISED NUMBERS 1 THRU 10.

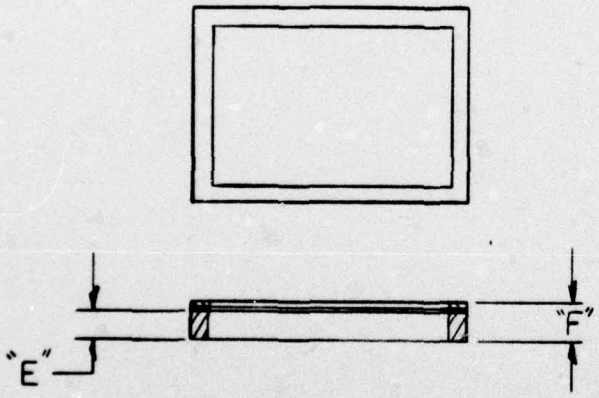
to prevent oxidation during the glass sealing operation. The corral assembly is depicted in figure 3-3. Materials and dimensioning specifications for the ceramic corral, metal frame, brazing alloy preform and metal cover were previously reported [ref. 5].

The ceramic corrals were purchased to a dimensional tolerance of $\pm$ 1%. The corrals were manufactured by dry-pressing and, as received, were mostly within the specified tolerance. In fact, about 80% of the parts exhibited a dimensional variation of less than 0.5% in the outside dimensions. The tight dimensional tolerancing was required to allow accurate fixturing for corral assembly. The brazing preforms were etched from copper-silver eutectic sheet stock.

Carbon fixtures were designed and built for use in properly locating the preform and frame with respect to the ceramic corral during the brazing process. Several fixturing methods and materials were tried. Aluminum oxide fixturing, which located the ring-shaped parts by their internal features, failed to hold dimensional tolerances. A boron nitride fixture was tried but spalled in the hydrogen brazing furnace. Carbon fixtures which locate by outside part features have been successful. The carbon brazing tray is shown in figure 3-4. Since the grade of carbon used has an expansion coefficient very similar to the Kovar frame and the alumina corral, the fixture clearances could be designed for parts based on their room- temperature dimensions.

Fixtures also were designed and fabricated (from Kovar) for use in properly aligning the corral assembly to the substrate during the glass- sealing process. This fixture is shown in figure 3-5. Figure 3-6 shows the final hybrid microcircuit assembly, with the corral assembly and cover in place. In attaching the corral assembly to the thick film substrate, first the ceramic bottom surface of the corral assembly is glassivated using a tape transfer process for affixing a glass preform to it and then sintering the glassivated assembly in a furnace at about 500°C, thus fusing the glass to the ceramic. The glass is a modified lead-zinc-borate devitrifiable solder glass with a thermal expansion coefficient reasonably well matched to the alumina.

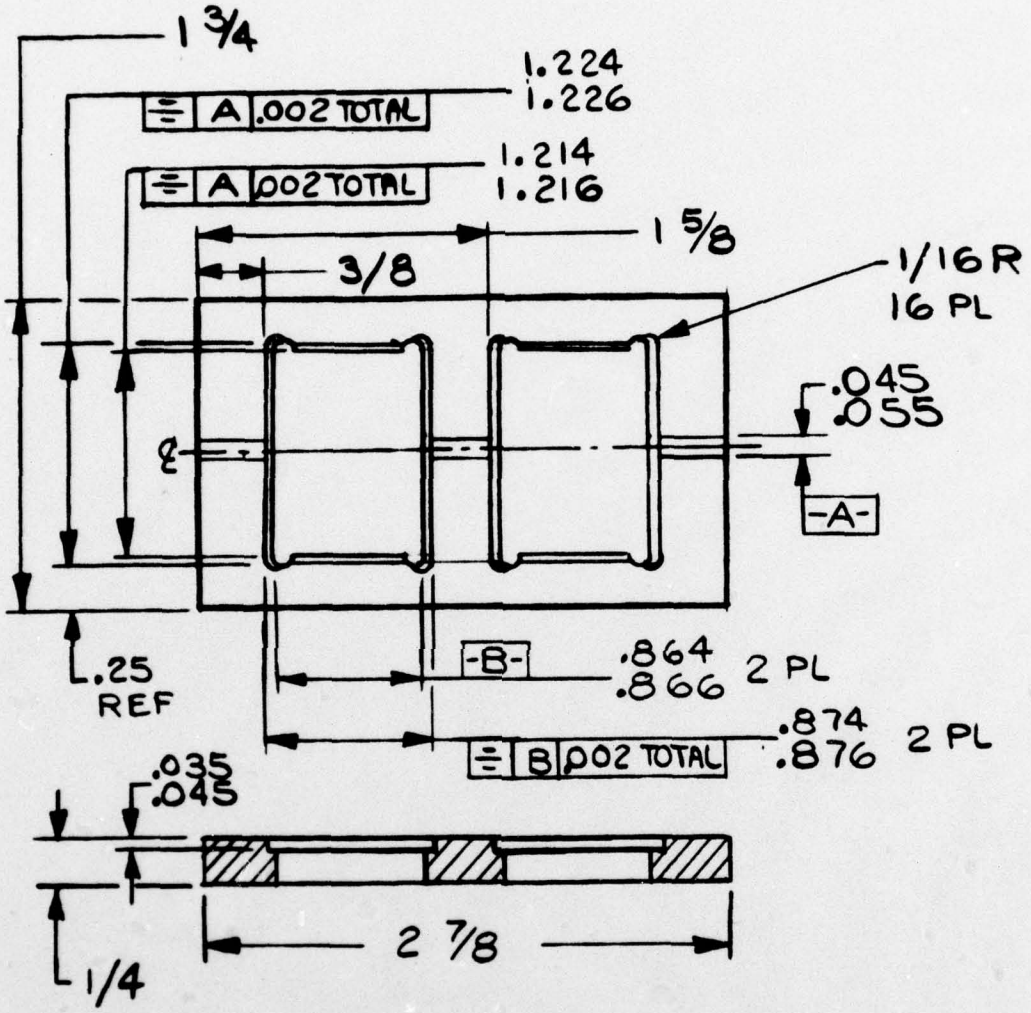



NOTE:

1. METALLIZED SURFACE
2. USE BRAZING TRAY FIXTURE NO. 31362 FOR ATTACHMENT TO CORRAL

**Figure 3-3. Corral Assembly**




NOTES
1. MATL: W-120 (L-56) CARBON
2. TOL: FRACTIONS ± 1/32

Figure 3-4. Brazing Tray for Corral Assembly

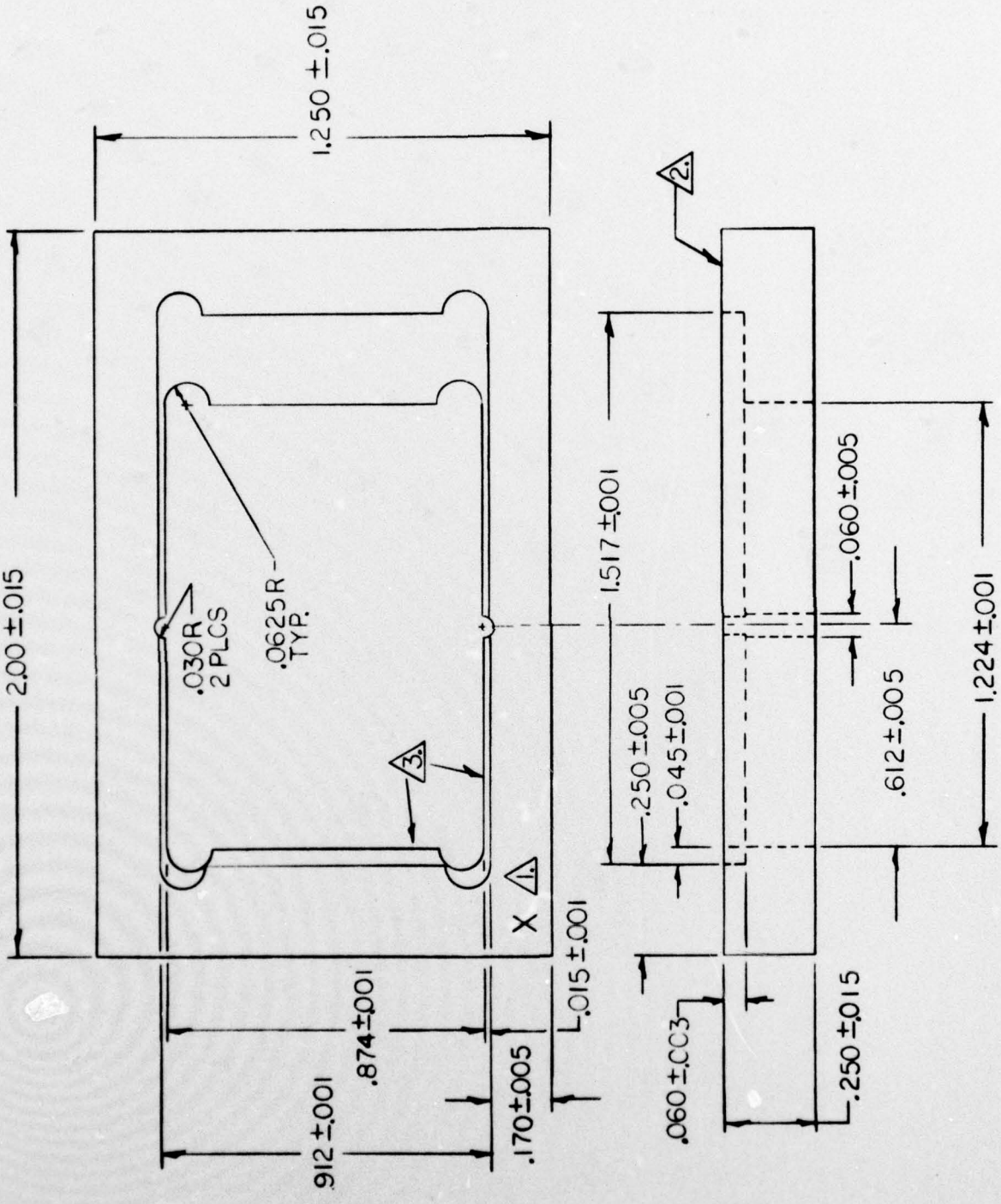



**Figure 3-5. Corral Alignment Fixture**

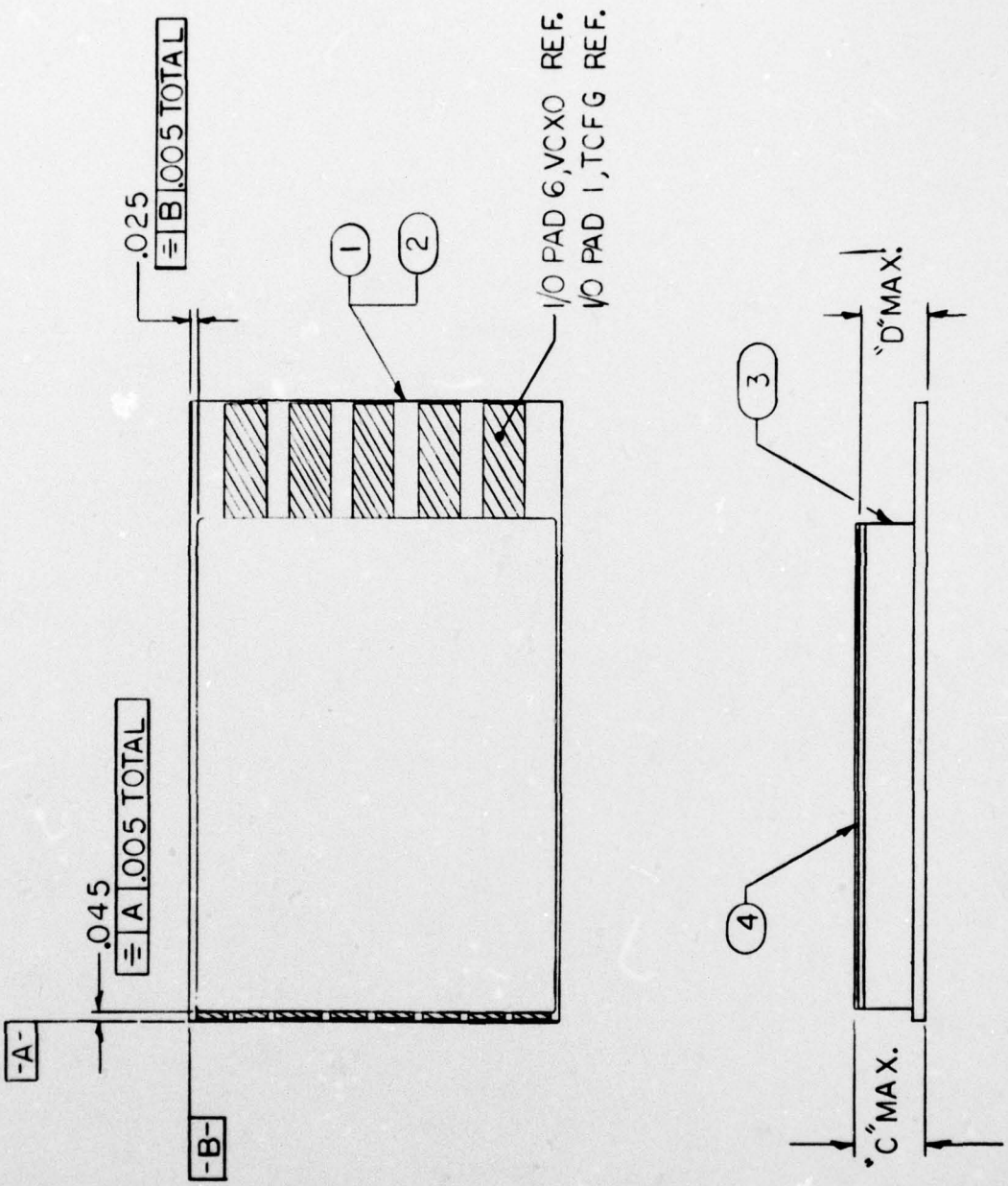



Figure 3-6. Final Hybrid Assembly

The corral-to-substrate attachment process can be performed in a belt furnace or using a hot plate. A high rate of temperature rise is required for the assembly in order to obtain low glass viscosity and good flow prior to devitrification. Corrals have been attached to substrates on a 500°C hot plate. The glass was allowed to devitrify for ten minutes. The hot-plate process works well and will be used in the fabrication of the engineering samples. In production, a belt furnace will be used.

Some preliminary work was performed on cover sealing. The covers and corral assemblies are designed to be parallel-seam welded together. Weld sealing was attempted on five samples using two different machines. Three samples were seam welded on a Raytheon seam welder with the following conditions constant:

| | |
|---|---|
| Electrode pressure | 2 lbs. |
| Sealing speed | 4 inches/minute |
| Pulse rate | 400/minute |
| Weld frequency | 1 cycle of 60 Hz = 11% duty cycle |

The welder heat setting was 22, 28 and 35 for the three units. The two units welded at the lower settings passed 1 x $10^{-8}$ He leak test, but the welds were judged to be marginal in quality.

The remaining two samples were welded on an SSEC seam welder, which has a 1000 Hz supply. The weld parameters used were as follows:

| | |
|---|---|
| Weld current (p-p) | 300 Amperes |
| Pulse width | 20 milliseconds |
| Pulse repetition time | 60 milliseconds |
| Sealing speed | 9.6 inches/minute |

The first welded sample was tested for gross leaks and passed. The second unit appeared visually identical to the first after sealing, however, a leak at the ceramic-to-glass seal was detected. The cover of this sample was removed in order to determine weld quality. The weld nugget was very pronounced and suggested that there was considerable margin available for reducing welding current level.

## 3.3 Test Flow Plan

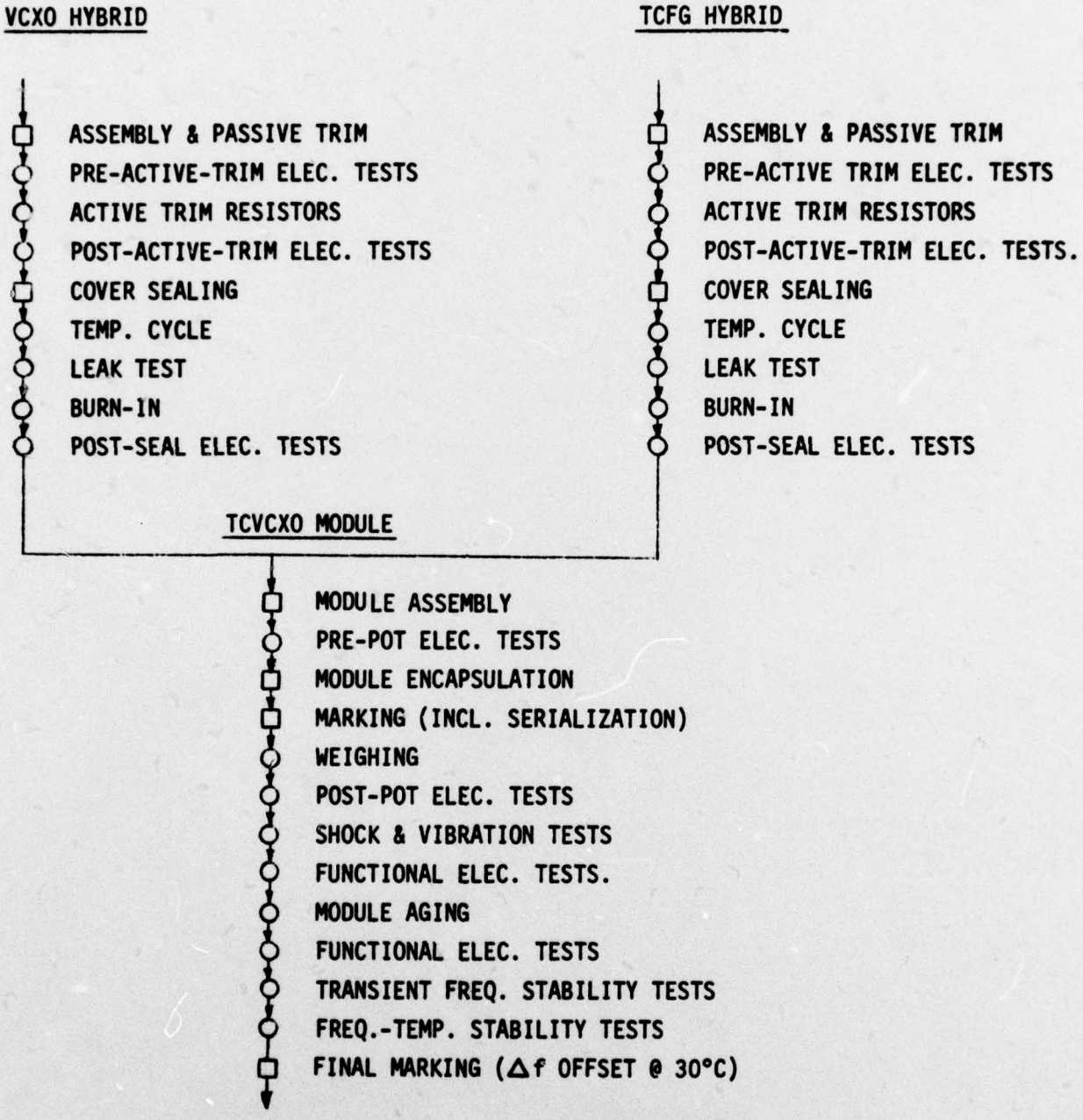
A detailed test flow plan was generated for the TCFG and VCXO substrate assemblies and for the TCVCXO module assemblies. The tests included in the flow plan are derived from ECOM Technical Requirements SCS-483 [ref. 3]. Table 3-1 lists the tests to be performed and provides a cross-reference between the applicable sections of ECOM Technical Requirements SCS-483, the military specification for crystal oscillators MIL-O-55310 and the military standard for testing electronic parts MIL-STD-202. These tests will be selectively applied at various levels of module assembly so as to optimize their effectiveness while minimizing production cost. In addition, several other tests, derived from the SCS-483 tests and from the functional resistor trim procedure will be used for in-process screening of the individual hybrid substrate assemblies. The overall test flow plan is presented in figure 3-7, and segments of it detailed in figures 3-8, 3-9 and 3-10.

The pre-active trim tests, cited in figures 3-7, 3-8 and 3-9 for the substrate assemblies, are intended to verify that all active components are functioning. The post-active trim tests, cited in these same figures, are intended to check the accuracy of the functional resistor trims and to check the basic performance of the assemblies at room temperature.

The pre-pot and post-pot electrical tests referred to in figure 3-7 are some of the functional tests listed in table 3-1. The pre-pot tests will consist of all of the electrical tests in table 3-1, except transient frequency stability, frequency-temperature stability and aging. These tests are delineated in figure 3-10. The post-pot tests will consist of only supply voltage, input power and RF output voltage checks. Functional electrical tests to be performed immediately prior to and following module aging will be the same as for pre-pot testing. Following aging, the transient frequency stability and frequency-temperature stability tests will also be performed on modules in production. As for the engineering samples, these tests will also be performed prior to aging so as to determine the effects of aging on these parameters.

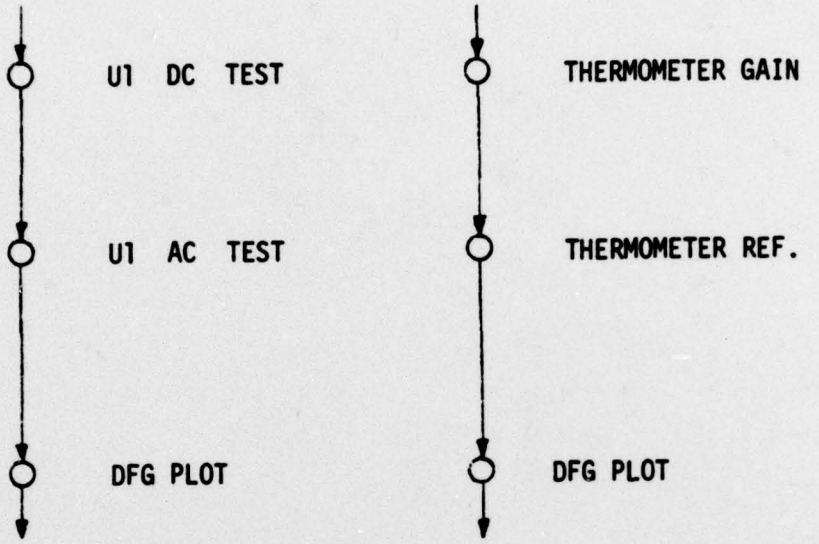
TABLE 3-1. TCVCXO TEST REQUIREMENTS

| TEST PARAMETER | TEST REQ. PARAGRAPH SCS-483 | TEST METHOD PARAGRAPH | | |
|---|---|---|---|---|
| | | SCS-483 | MIL-O-55310 | MIL-STD-202E |
| SEAL | 3.7 | 4.7 | | 112 A/C/IV |
| WEIGHT | 3.8 | 4.3 | - | - |
| FREQ. RANGE | 3.9 | 4.3 | - | - |
| FREQ.- TEMP. STABILITY | 3.10 | 4.8 | 4.8.8.1 | - |
| FREQ.- VOLT. STABILITY | 3.11 | 4.3 | - | - |
| FREQ.-LOAD STABILITY | 3.12 | 4.3 | - | - |
| TRANS. FREQ. STABILITY | 3.13 | 4.3 | - | - |
| AGING | 3.14 | 4.9 | 4.8.29 | - |
| SHOCK | 3.15 | 4.10 | - | 213 A/E |
| VIBRATION | 3.16 | 4.11 | - | 204 B/B |
| FREQ. ADJUST | 3.17 | 4.12 | 4.8.9 | - |
| MODULATION $V_{in}$ | 3.18 | 4.13 | 4.8.4.3 | - |
| MOD. $Z_{in}$ (ANALOG) | 3.19 | 4.14 | 4.8.5 | - |
| FREQ. DEVIATION | 3.20 | 4.15 | 4.8.25 | - |
| DEV. LINEARITY (ANALOG) | 3.21 | 4.16 | 4.8.27 | - |
| SUPPLY VOLTAGE | 3.22 | 4.17 | 4.8.4.1 | - |
| INPUT POWER | 3.23 | 4.18 | 4.8.6.1 | - |
| OUTPUT VOLTAGE | 3.24 | 4.19 | 4.8.12.1 | - |
| MARKING | 3.25 | 4.20 | 3.8 | - |




NOTE: □ Denotes fabrication step, ○ denotes test step.

FIGURE 3.7 TCVCXO TEST FLOW PLAN




a) Pre-Functional Trim Tests

b) Post-Functional Trim Tests

NOTE: DFG PLOT = Plot of Diode Function Generator Output Voltage.

Figure 3-8. TCFG Hybrid Tests

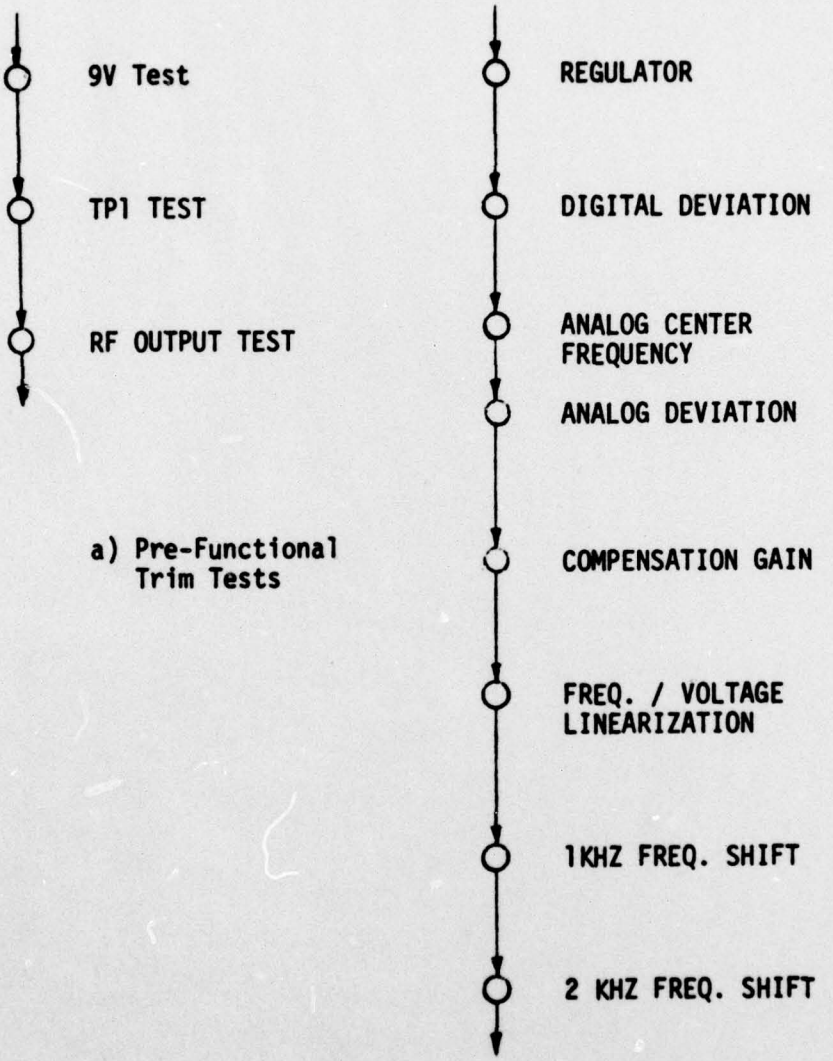



Figure 3-9. VCXO Hybrid Tests

TEST #1 - INPUT POWER (Ref. 3.22, 3.23)

TEST #2 - RF OUTPUT (Ref. 3.24)

TEST #3 - FREQ. VOLTAGE STABILITY (Ref. 3.11)

TEST #4 - FREQ. - LOAD STABILITY (Ref. 3.12)

TEST #5 - ANALOG INPUT IMPEDANCE (Ref. 3.19)

TEST #6 - ANALOG FREQ. DEVIATION
(Ref. 3.9, 3.17, 3.20. 3.21)

TEST #7 - FSK DEVIATION (Ref. 3.18, 3.20)

NOTE: Reference nos. are to paragraphs in
ECOM Technical Requirement SCS-483

Figure 3-10. TCVCXO Module Functional Tests

3.4 Test Procedures

Preparation of the following test procedures were started for use in TCVCXO module production:

a) TCFG Functional - This procedure will describe the go/no go tests for TCFG substrate assemblies prior to functional resistor trimming and the post-functional-trim tests designed to check the accuracy of the trims accomplished as well as to serve as a post-burn-in test for the TCFG hybrids. These are the tests outlined in figure 3-8.

b) VCXO Functional - This procedure will describe the go/no-go tests fpr VCXO substrate assemblies prior to functional resistor trimming and the post-functional-trim tests designed to check the accuracy of the trims as well as to serve as a post-burn-in test for the VCXO hybrids. These are the tests outlined in figure 3-9.

c) TCVCXO Functional - This procedure will describe all of the room-temperature electrical tests to be performed on the module assemblies, except transient frequency stability. These tests will be conducted after module assembly, after potting (in part), after shock and vibration and after aging. These tests are outlined in figure 3-10.

d) TCVCXO Transient Frequency Stability - This procedure will describe the test for transient frequency stability of the TCVCXO at power turn-on and will be performed in production after module aging, and for engineering samples, will be performed both before and after module aging. A discussion of the set-up for this test is presented below in 3.4.1.

e) TCVCXO Temperature Stability - This procedure will describe the process for functional laser trimming of resistors in TCFG substrate assemblies and will be derived from ECOM's procedure as presented in the first quarterly report. [Ref. 6]

g) VCXO Functional Trim - This procedure will describe the process for functional laser trimming of resistors in VCXO substrate assemblies and will be derived from ECOM's procedure as presented in the first quarterly report. [Ref. 6]

Details contained in the above-listed procedures will be covered in future reports. The documents are currently in draft form and are being refined based on experiences in their usage during the engineering phase.

3.4.1 Turn-On Stability Test Set-Up - A measurement scheme for transient frequency stability has been configured around the HP 5360A computing counter and the HP 5375A programmer, whereby three frequency measurements can be made and stored at any three instants following application of supply power to the TCVCXO. In particular, these measurements can be selected in the time interval from 5 ms to 100 ms after turn-on as specified in SCS-483, paragraph 3.13. A block diagram of the test set-up is shown in figure 3-11.

A function generator is used to trigger the 12V supply and a pulse generator simultaneously. The pulse generator can be set to delay its output 5 ms and, by properly setting the repetition rate, a pulse can be made to occur 95 ms later or at the end of any other interval desired. These pulses feed the programmer, which in turn activates the counter at the pulse interval times. The measured values can be read out at the end of the test. This scheme can be implemented for fully automatic measurement in a production set-up.

This scheme for measuring transient frequency stability at turn-on was developed and evaluated using the TCVCXO discrete-component breadboard as the unit-under-test. The resulting measurement data is shown in table 3-2.

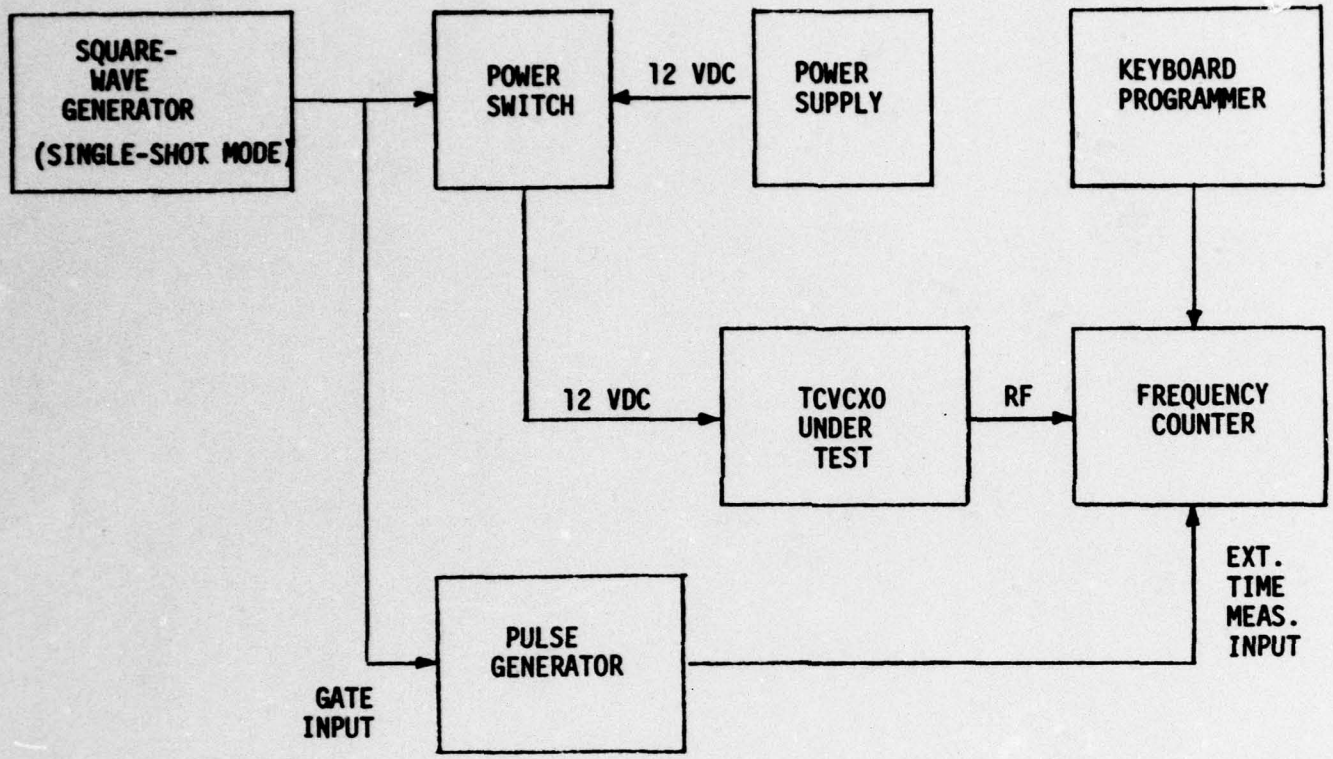



FIGURE 3-11. BLOCK DIAGRAM - TRANSIENT FREQUENCY STABILITY TEST SET-UP

TABLE 3-2. TRANSIENT FREQUENCY STABILITY TEST DATA ON TCVCXO BREADBOARD

| Sample Time (msec.) | 100 | 300 | 500 |
|---|---|---|---|
| | 116.2 | 116.6 | 117.1 |
| | 114.9 | 115.5 | 116.0 |
| | 114.8 | 115.5 | 115.7 |
| | 115.1 | 115.8 | 116.7 |
| | 115.7 | 115.3 | 115.8 |

| Sample Time (msec.) | 50 | 100 | 150 |
|---|---|---|---|
| | 114.9 | 115.3 | 115.8 |

| Sample Time (msec.) | 20 | 60 | 80 |
|---|---|---|---|
| | 114.0 | 114.0 | 114.9 |
| | 113.7 | 114.8 | 114.6 |
| | 113.3 | 114.8 | 114.2 |
| | 113.1 | 114.2 | 114.6 |

| Sample Time (msec.) | 5 | 48 | 88 |
|---|---|---|---|
| | 114.0 | 114.6 | 115.1 |
| | 114.2 | 114.8 | 115.5 |

NOTE: Frequency measured is 17,999,XXX.X Hz and only last four digits are shown above.

## 4.0 FIXTURING AND TOOLING

This section covers the work performed on the following tasks:

Task no. 11 - Thick film printing screen procurement

Task no. 20 - Test fixture design and fabrication

Additional fixturing and tooling has been designed and fabricated for use in the hermetic sealing process, and was discussed in section 3.2 of this report.

### 4.1 Thick Film Screens

Standard 325-mesh, stainless-steel wire screens were purchased for use in printing the various thick film patterns onto the substrates. One set each of seven screens was purchased for the TCFG and VCXO design types. Each screen pattern corresponded to one of the artwork patterns shown in figures 2-5 through 2-18.

### 4.2 Test Fixturing

The test fixturing on which work has been accomplished consists of fixturing for passive and functional resistor trimming, and fixturing for electrical testing of microcircuits and modules.

4.2.1 Resistor Trimming Fixturing - The special fixturing required for resistor trimming includes the following:

- Probe cards, passive resistor trim
  - TCFG hybrid (2)
  - VCXO hybrid (2)
- Probe cards, functional resistor trim
  - TCFG hybrid (1)
  - VCXO hybrid (1)
- Substrate holding fixture

Because of the large number of resistors to be trimmed per module (60 in the TCFG and 45 in the VCXO), and the very high substrate circuit density, it was decided from the start to build fixed probe cards for passive and functional resistor trimming. Three major factors influenced the design of these probe cards. First, the configuration of the laser trimmer to be used dictates that the substrate surface be 0.800 inch below the top of the probe card, an unusually large spacing that can lead to problems with alignment and with a probe scrubbing action on the substrate. Secondly, because of resistor value shifting

during corral-to-substrate attachment (a 500°C process), it is highly desirable that resistors be trimmed to value after corral attachment. Therefore, the probe needles must be long enough to clear a 0.140 inch (worse case) corral and still contact the substrate accurately. These two factors in combination preclude the use of a standard probe design. A special probe arm and needle are being designed and fabricated by a major probe card vendor to meet these depth and clearance requirements.

The third factor affecting probe card design is the existence of a large number of closed resistor loops in the two hybrids and especially in the TCFG. The trimming of resistors in closed loops requires the use of guard probes to isolate electrically the resistor being trimmed from those paths paralleling it. Thus, the very high resistor count coupled with the need for guard probes results in a very high probe count for each hybrid design type. Consequently, two different probe cards will be necessary for the passive resistor trimming of each substrate type. Only one card per type will be needed for functional trimming however, due to the relatively low number of resistors to be so trimmed.

A special substrate holding fixture is also needed for resistor trimming, and again it is due to the corral clearance problem. The laser trimmer normally allows only a 0.100 inch probe card travel in the Z-axis. Therefore, the 0.150 inch long probe needles cannot be raised enough to allow a corralled substrate to be slipped into trimming position, without trimmer modification. To solve this problem, an "elevator" fixture was designed and built. This fixture has two vertical positions, the first being trimming height and the second, 0.250 inch lower, for corral clearance. With this modification, the substrate will be loaded at the lower position, swung under the probe needles and then raised into the probe contact position for trimming purposes. The upper position is made precise, since the laser's target must be accurately located in the Z-direction to $\pm$ 1 mil for good trimming results.

Fixed probe cards will not be available for use on the first lot (10-lot) of engineering samples due to a long lead-time required to build the special probes described above. These first substrates will be trimmed with manually set adjustable probes. Each such probe must be aligned manually and secured to a probe support ring. This is a time-consuming and tedious process, since circuit densities dictate at least three such set-ups of 10-15 probes each per set-up for passive trim of each substrate type. Then each set-up must be torn down after use for probe and probe ring re-use. This process is not cost effective for production use but will be implemented on the first lot of engineering samples so that the lead time for custom fixed probe cards will not gate their fabrication.

4.2.2 Electrical Testing Fixturing - The special fixturing required for electrical testing of substrate assemblies, unsealed and sealed, and module assemblies includes the following:

- Probe card, hybrid functional electrical test
- Test fixture, hybrid functional
- Test box, functional
- Electronic switch

The proper testing of hybrid substrate assemblies requires that several points in the circuit be addressed besides those available at the external connector contact pads. Consequently, a probing set-up has been devised, consisting of a probe card and a substrate holding fixture. The holding fixture will be an aluminum block with recessed nests in which will rest the substrate assemblies and a PC-board edge connector which will slip onto the ends of the substrates having the contact pads. The two hybrid types will sit side-by-side on the holding fixture. The fixture will be placed on a probing machine where a fixed-point probe card will address key points in the circuits and provide the appropriate electrical interconnections between the two hybrid types. Thus the substrate assemblies can be electrically tested individually or as a complete module function

prior to cover sealing and module assembly.

The probe card and connector in the fixturing described above will be wired to a functional test box which will contain the switching, circuitry, loads and connectors required to completely test the TCVCXO module and TCFG and VCXO substrate assemblies at room temperature (except for transient frequency stability testing, which is a different set up). This test box has been designed and its schematic is shown in figure 4-1.

The requirement for an electronic switch results from the fact that SCS-483 dictates that frequency measurements be made continuously over the temperature range at center frequency and at each of the deviation limits. Details on the design and construction of this switch will be covered in the next quarterly report.

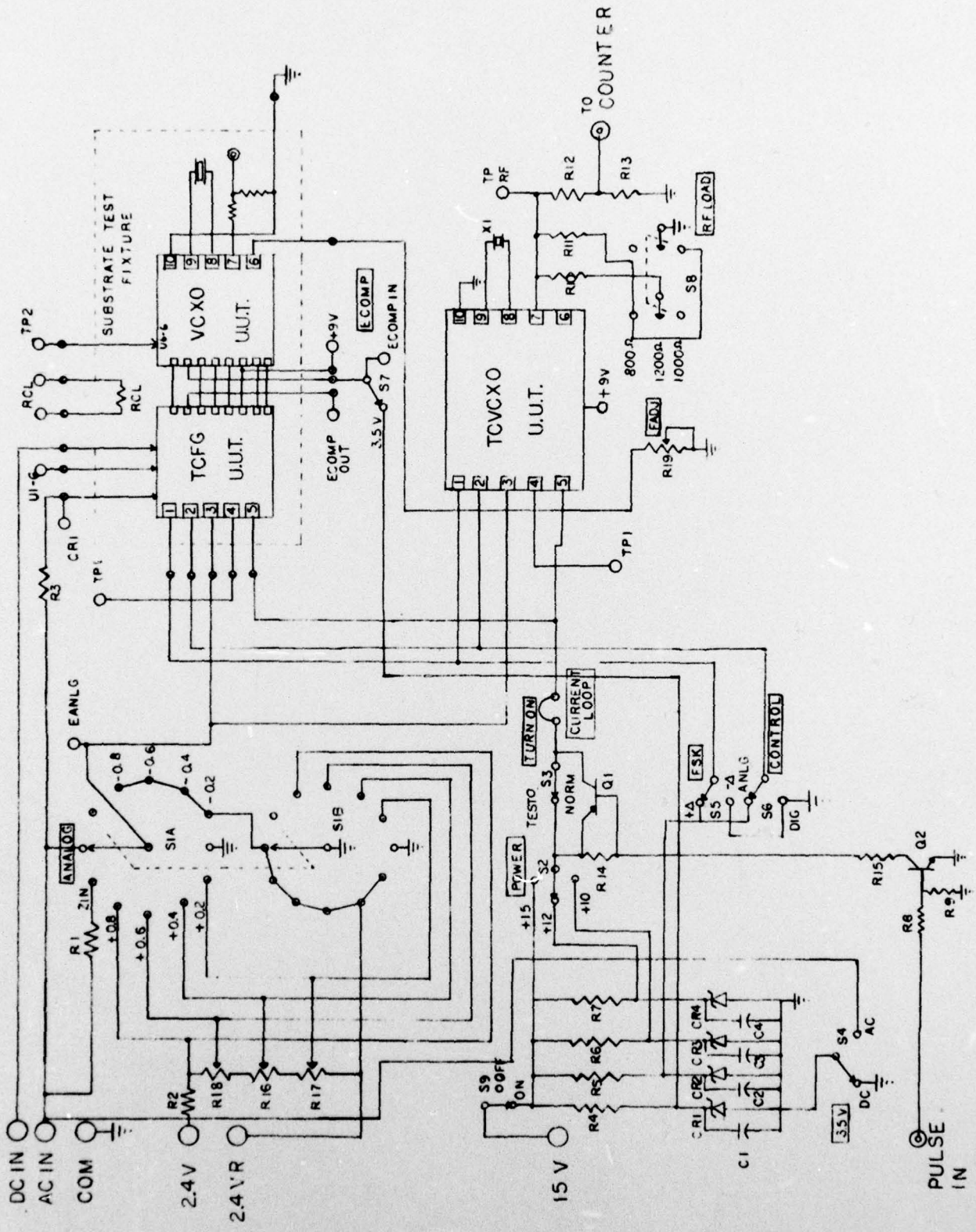



Figure 4-1. Schematic Diagram of Functional Test Box

## 5.0 MANUFACTURING

This section covers the work performed on the following tasks:

Task no. 21 - Thick film substrate fabrication

Task no. 22 - Substrate assembly (10-lot)

### 5.1 Thick Film Substrate Fabrication

The thick film processing of the substrates for the TCFG and VCXO hybrids was accomplished following the procedure previously delineated, [Ref. 7]. The thick film materials used were Plessey C6010 for the platinum-gold first conductor pattern, DuPont 9910 for the gold overlay and 1400 series Birox for the resistor patterns. Some problems were experienced with achieving good geometrical definition in the printed resistors, due to their large number and small size and the substrate camber, which was a standard 4 mils per linear inch.

Figures 5-1 and 5-2 are photographs of the screened-and-fired TCFG and VCXO thick film substrates, respectively.

### 5.2 Substrate Assembly

Included in this task are the following sequential operations: corral assembly, corral-to-substrate attachment, passive resistor trimming, component assembly and functional resistor trimming. During this quarter, the following assembly operations were completed for the first lot (i.e., 10-lot) of engineering samples: corral assembly for the TCFG and VCXO hybrids and glass-sealing of corral assemblies to TCFG substrates. Figure 5-3 is a photograph of the brazing fixture and piece-parts used in corral assembly. Figure 5-4 is a photograph of the alignment fixture used in corral attachment and shows the substrate and corral assembly in position for glass sealing. Figure 5-5 shows some corral assemblies and a corral assembly sealed to a TCFG substrate.

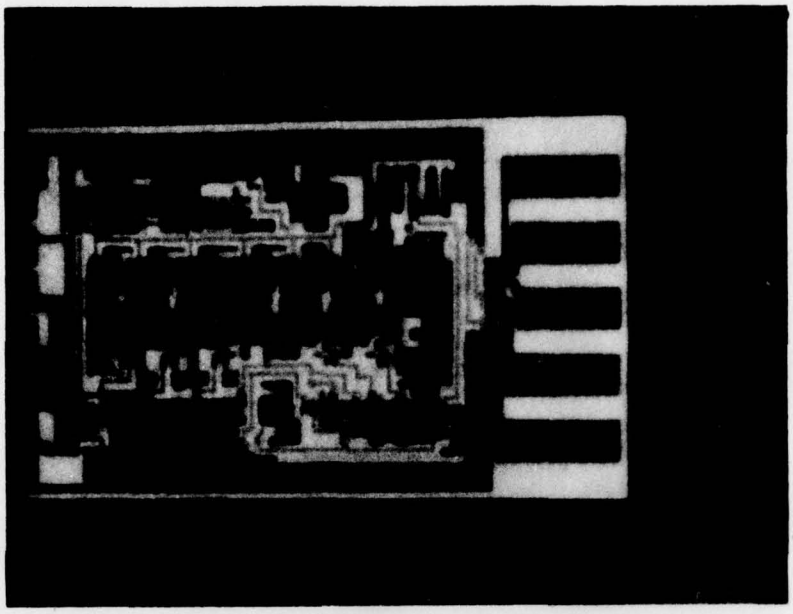


Figure 5-1. TCFG Thick Film Substrate

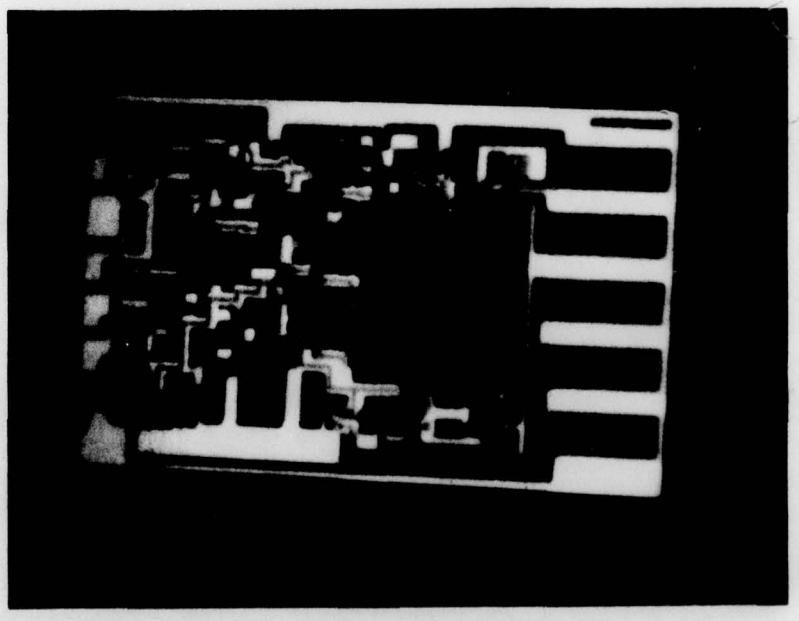


Figure 5-2. VCXO Thick Film Substrate

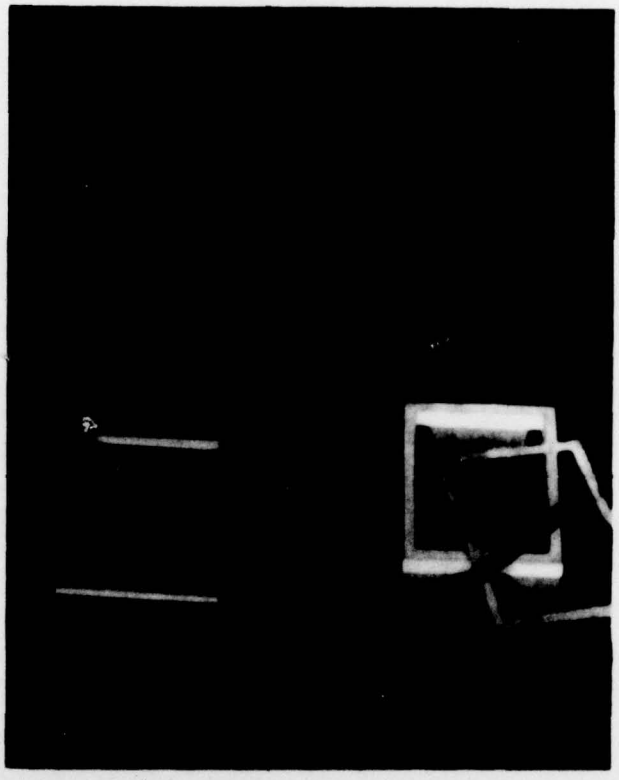


Figure 5-3. Corral Assembly Fixturing and Piece-Parts

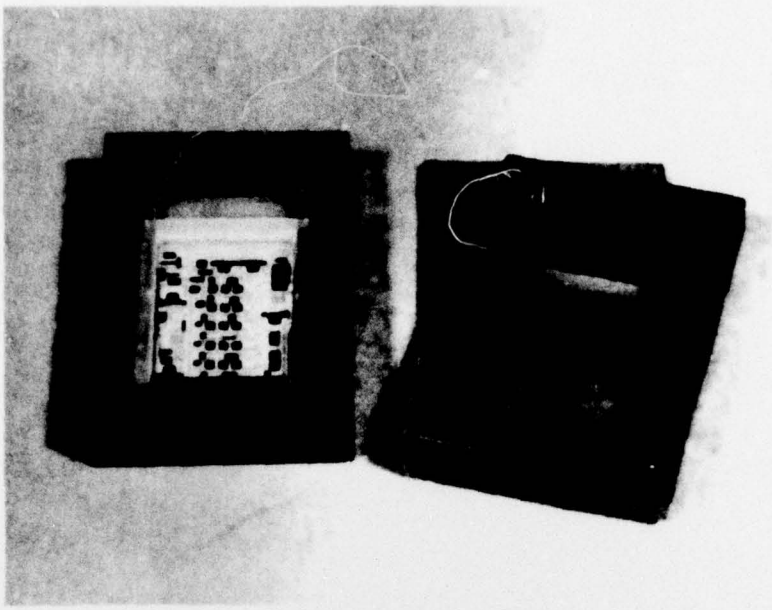


Figure 5-4. Corral Attachment Fixturing and Piece-Parts.

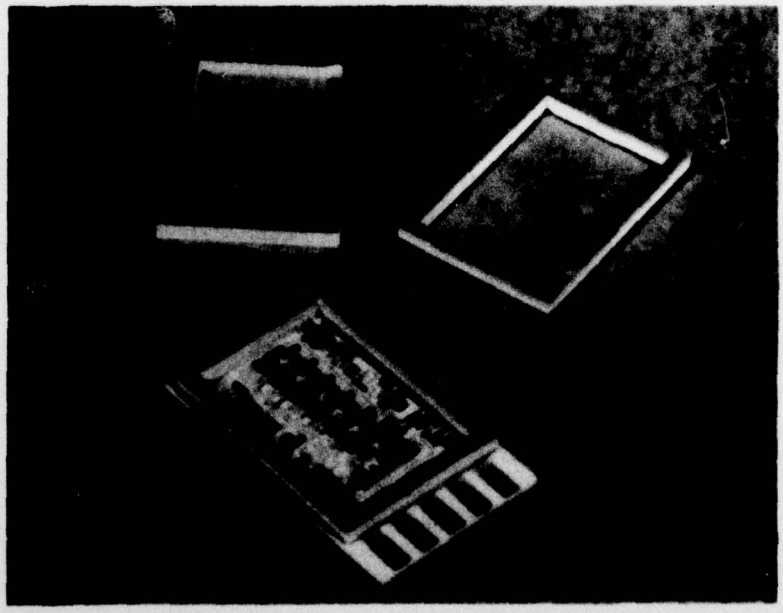


Figure 5-5. Corrals Assembled and Attached

## 6.0 CONCLUSION

The major accomplishments during the second quarter of this program have been the addition to the module configuration design of a module extraction feature, the detailed design of a module potting shell, the generation of a set of master artwork for each of the TCVCXO's two hybrid design types (i.e. TCFG and VCXO), the continued development of a process for hermetically sealing the hybrid microcircuits, the generation of detailed test flow plans and preliminary electrical test procedures for the module and constituent hybrids, the design and fabrication of special tooling and fixturing for hermetically sealing, resistor trimming and electrical testing,the processing of TCFG and VCXO thick film substrates and the start of TCFG substrate assembly. Efforts to date have shown that the key areas of concern so far in the manufacturing process are resistor trimming and cover sealing. The resistor trimming concern pertains to the necessity for using probe cards which are of a very high density and which must use special long-needle probes of an unproven design. The cover sealing concern pertains to the lack of success to date in achieving hermetic cover seals to the corral with a high yield. Future efforts will be devoted to both areas to ensure that they do not adversely effect TCVCXO manufacturability.

## 7.0 PROGRAM FOR NEXT QUARTER

During the next reporting period, work will be concluded on the development of the hermetic sealing process, the generation of electrical test procedures, the fabrication of test fixtures, the assembly of substrates for the 10-lot of engineering samples, the hermetic sealing and leak testing of the 10-lot engineering samples, and the assembly and electrical testing of the 10-lot modules. Aging of the 10-lot modules is also scheduled to begin, as is the development of the module encapsulation process.

## 8.0 REFERENCES


1. Raytheon Company, Quincy, Mass., MANUFACTURING METHODS AND TECHNOLOGY ENGINEERING (MM&TE) PROGRAM FOR THE ESTABLISHMENT OF PRODUCTION TECHNIQUES FOR HIGH DENSITY THICK FILM CIRCUITS USED IN CRYSTAL OSCILLATORS, First Quarterly Progress Report, 6 August 1976 - 21 November 1976, C. T. Martin, 30 December 1976 (Contract no. DAAB07-76-C-8119), Section 4.1.
2. Op. cit., Figures 17 and 18
3. Op. cit., Appendix A
4. Op. cit., Figure 4
5. Op. cit., Figures 5, 6, 7 and 8
6. Op. cit., Appendix B
7. Op. cit., Figures 11 and 12

# APPENDIX A

# IDENTIFICATION OF PERSONNEL

## IDENTIFICATION OF PERSONNEL

The following Raytheon Equipment Development Laboratories professional personnel performed work on this program during the second quarter. The man-hours of work performed by each individual is reported, as is the program contributions and technical background of each.

| | |
|---|---|
| Charles T. Martin* (177 hrs.) | TCVCXO Engineering Phase Project Manager; also prepared engineering phase monthly technical and second quarterly reports. |
| Leland Woodworth* (11 hrs.) | Prepared TCVCXO engineering phase monthly cost reports and supervised production control activity for TCVCXO parts and materials procurement |
| Stanley Czerepak* (99 hrs.) | Accomplished detailed design of piece-parts for TCVCXO encapsulation and generated master artwork for thick film screen procurement |
| Richard Colson* (68 hrs.) | Participated in generation of test flow plans and electrical test procedures for TCVCXO fabrication. |
| Richard Bemis* (36 hrs.) | Performed TCVCXO electrical bread-board testing in support of test pro-cedure generation effort. |
| Charles Morris* (68 hrs.) | Participated in generation of test flow plans and electrical test procedures and designed special tooling for electrical testing and resistor trimming of TCVCXO. |
| Joseph Malatino* (144 hrs.) | Performed thick film process development and processing of thick film substrates for TCVCXO<br>B.S. Physics, Sr. Engineer, Microcircuit Processing Section, responsible for thick film process development and operation of thick film processing lab facility. |
| Thomas Salzer (4 hrs.) | Supervised TCVCXO hermetic sealing process development and design of TCVCXO potting shell.<br>A.S.M.E., B.E.T. Mech. Eng., Principal Engineer in Microcircuit Engineering Section, responsible for hybrid assembly and packaging process development. |
| John Keohane (360 hrs.) | Performed TCVCXO hermetic sealing process development and participated in design of TCVCXO potting shell<br>B.A. Math. & Science, Sr. Engineer & Consultant to Microcircuit Engineering Section in hermetic glass sealing. |

* See first quarterly report for technical background.

The above listed personnel were assisted by the following support functions at the level of effort indicated:

| | |
|---|---|
| QC engineering | 17 hrs. |
| QC inspection | 21 hrs. |
| Electrical technician | 66 hrs. |
| Production control | 86 hrs. |
| Manufacturing | 60 hrs. |
| Machine shop | 37 hrs. |
| Drafting | 51 hrs. |
| Clerical | 28 hrs. |
| Supervision & Administration | 22 hrs. |
| Miscellaneous | 16 hrs. |

Total level of effort for this quarter was 1371 hrs.

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Bliley Electric Company
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Erie, PA 16512
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Sandwich, IL 60548
001 R. Hostetler

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001 J.L. Denman

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